# Figure. 01

# **Basic Logic Gates with Truth Table**





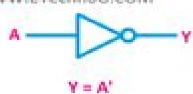
Boolean

Expression:

1	u	u	Ľ	Γa	D)	e	Š
	_	_	_	_	_		7

INPUT A	OUTPUT (Y)
0	0
1	1

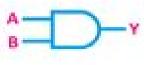
NOT Gate WWW.ETechnoG.COM



INPUT OUTPUT
A (Y)
0 1
1 0

INI	PUT .	OUTPUT	
A	8_	(Y)	
0	0	0	
0	1	0	
1	0	0	
1	1	1	

### **AND Gate**



Y = A . B

INF	PUT	OUTPUT	
A	В	(Y)	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

## **NAND** Gate



 $Y = A \cdot B$ 

## OR Gate



INF	UT	OUTPUT	
A	8	(Y)	
0	0	0	
0	1	1	
1	0	1	
1	1	1	

### **NOR Gate**



		-	
70.0	_	400	

IN	PUT	OUTPUT
A	8	(Y)
0	0	1
0	1	0
1	0	0
1	1	0

### **XOR Gate**

INI	PUT .	OUTPUT
A	8	(Y)
0	0	0
0	1	1
1	0	1
1	1	0

and the second
WWW.ETer mod COM.
B—//

		100	
-	-0.0		100
		100	-

INI	PUT	OUTPUT	
A	В	(Y)	
0	0	1	
0	1	0	
1	0	0	
1	1	1	

## **XNOR Gate**



Y = A + B

## **Logic Design Study Guide**

Jeffrey S. Brown, Susan L. Thomas, J. Peter Bruzzese

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