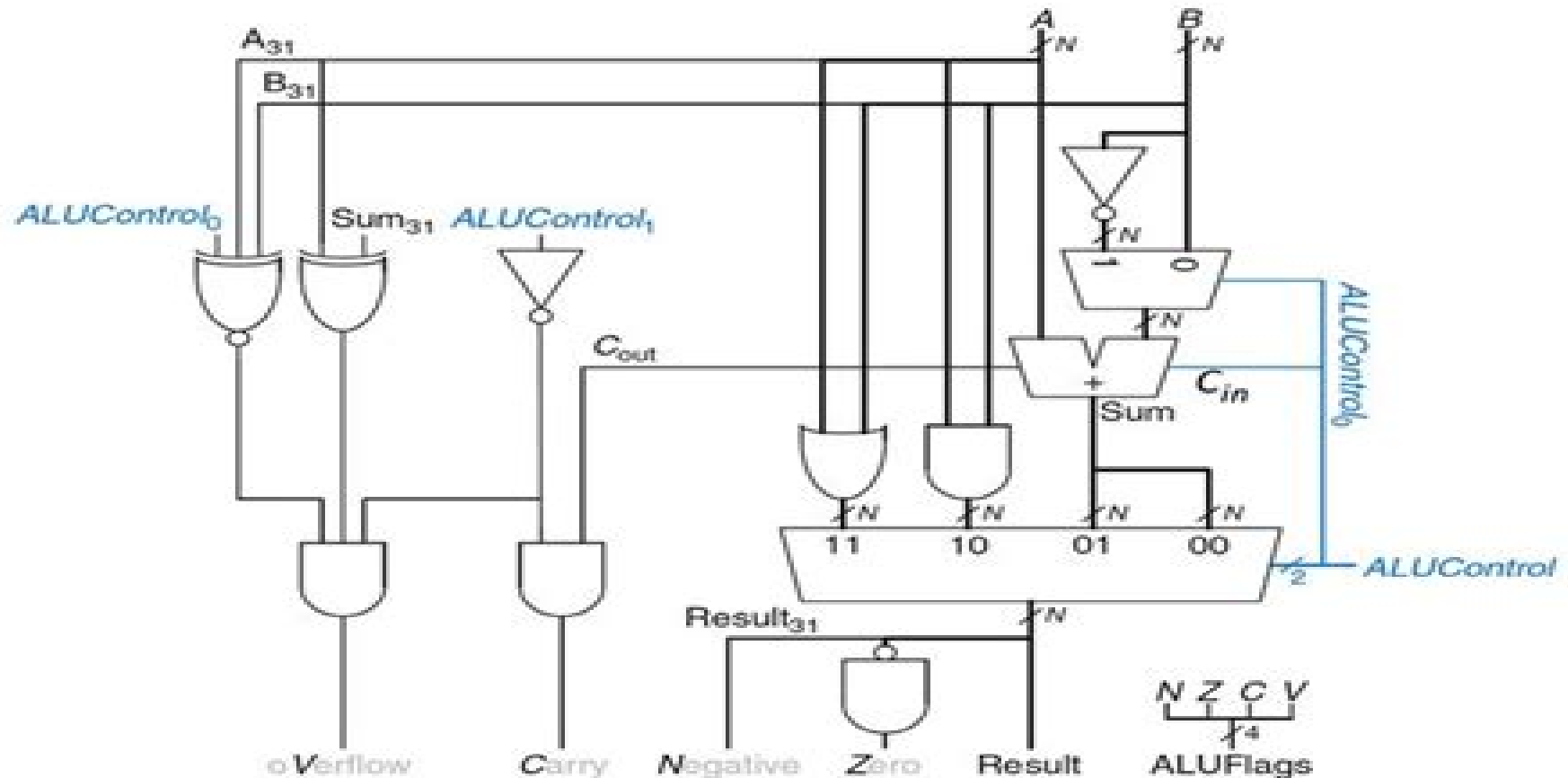


```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity ALU is
    Generic ( data_size : positive := 32 );
    Port ( A : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
          B : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
          ALUControl : in STD_LOGIC_VECTOR (1 downto 0);
          Result : out STD_LOGIC_VECTOR (data_size-1 downto 0);
          ALUFlags : out STD_LOGIC_VECTOR (3 downto 0));
end ALU;

```



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LM Reder



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