PDIP

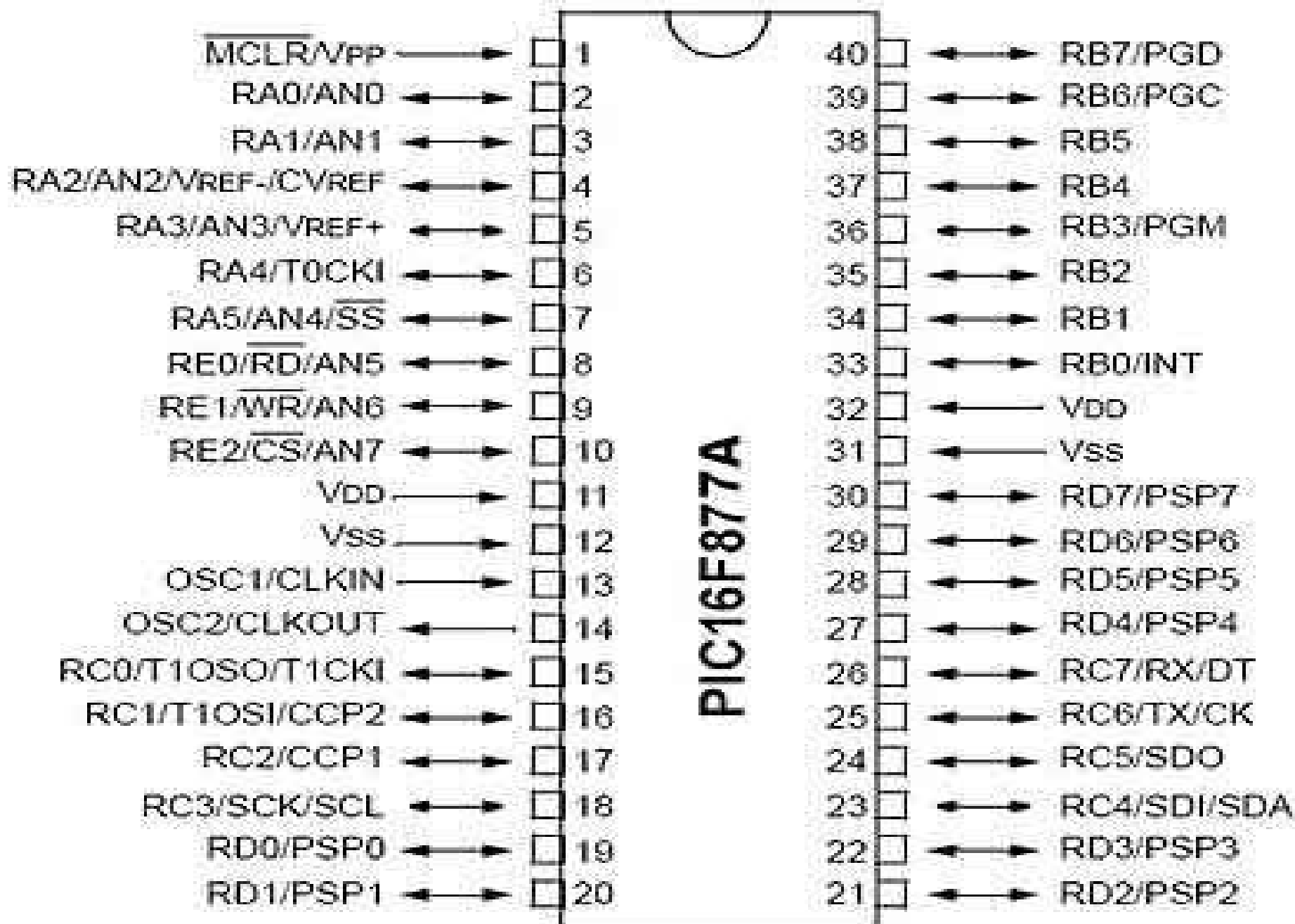|			
$\overline{\text{MCLR}}$/Vpp	→	1	40	RB7/PGD
RA0/AN0	→	2	39	RB6/PGC
RA1/AN1	→	3	38	RB5
RA2/AN2/VREF-/CVREF	→	4	37	RB4
RA3/AN3/VREF+	→	5	36	RB3/PGM
RA4/T0CKI	→	6	35	RB2
RA5/AN4/$\overline{\text{SS}}$	→	7	34	RB1
RE0/$\overline{\text{RD}}$/AN5	→	8	33	RB0/INT
RE1/$\overline{\text{WR}}$/AN6	→	9	32	VDD
RE2/$\overline{\text{CS}}$/AN7	→	10	31	VSS
VDD	→	11	30	RD7/PSP7
VSS	→	12	29	RD6/PSP6
OSC1/CLKIN	→	13	28	RD5/PSP5
OSC2/CLKOUT	→	14	27	RD4/PSP4
RC0/T1OSO/T1CKI	→	15	26	RC7/RX/DT
RC1/T1OSI/CCP2	→	16	25	RC6/TX/CK
RC2/CCP1	→	17	24	RC5/SDO
RC3/SCK/SCL	→	18	23	RC4/SDI/SDA
RD0/PSP0	→	19	22	RD3/PSP3
RD1/PSP1	→	20	21	RD2/PSP2

PIC16F877A

Lab Manual For Pic 16f877a Microcontroller

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