

QUESTION PAPER CODE : 11343
B.E./B.TECH. DEGREE EXAMINATION,
NOVEMBER/DECEMBER 2012.

Sixth Semester
Electronics and Communication Engineering
EC 2354/EC64—VLSI DESIGN
(Regulation 2008)

(Common to PTEC 2354—VLSI Design for B.E. (Part-Time)
Fifth Semester-Electronics and Communication
Engineering-Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A—(10 × 2 = 20 marks)

1. Why the tunneling current is higher for NMOS transistors than PMOS transistors with silica gate?
2. What is the objective of layout rules?
3. Give the effect of supply voltage and temperature variations on the CMOS system performance.
4. What are the factors that cause static power dissipation in CMOS circuits?
5. State the reasons for the speed advantage of CVSL family.
6. Mention the qualities of an ideal sequencing method.
7. Distinguish testers and test fixtures.
8. What are the stages at which a chip can be tested?
9. Write the Verilog module for a 1-bit full adder.
10. Give an example for implicit continuous assignment.

PART B—(5 × 16 = 80 marks)

- 11.(a)(i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (10)

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Basic Electronics Rakesh Kumar Garg, Ashish Dixit, Pavan Yadav, 2008 **VLSI-SoC: Design for Reliability, Security, and Low Power** Youngsoo Shin, Chi Ying Tsui, Jae-Joon Kim, Kiyoungh Choi, Ricardo Reis, 2016-09-12 This book contains extended and revised versions of the best papers presented at the 23rd IFIP WG 10.5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2015 held in Daejeon Korea in October 2015. The 10 papers included in the book were carefully reviewed and selected from the 44 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about new challenges both at the physical and system design levels as well as in the test of these systems.

Low-Power CMOS Design Anantha Chandrakasan, Robert W. Brodersen, 1998-02-11 This collection of important papers provides a comprehensive overview of low power system design from component technologies and circuits to architecture system design and CAD techniques. LOW POWER CMOS DESIGN summarizes the key low power contributions through papers written by experts in this evolving field. *Digest of Technical Papers*, 1999. *Proceedings, 1997 International Symposium on Low Power Electronics and Design* IEEE Circuits and Systems Society, 1997. VLSI Design 2001 : Fourteenth International Conference on VLSI Design VLSI Society of India, 2001. The International Conference on VLSI Design was started in 1985 as a workshop and from this start has grown into an international conference on VLSI design. The proceedings are dedicated to all aspects of integrated circuit design technology and related computer aided design CAD.

A Handbook On Multidisciplinary Approaches In Research (Volume-1) Er. Sandeep Bishla, Dr. Sahab Ram Kumawat, 2023-04-28 This chapter has a dual purpose. In the first place the authors provide a real world example of interdisciplinary research by discussing the two chapter examples they worked on while editing a book full of multidisciplinary cases. The authors purpose is to provide a realistic picture of how the theoretical aim of interdisciplinary research might be realised in practise in contrast to the numerous theoretical descriptions that have been published on the topic. The author gives the present conceptual understanding of the multidisciplinary before elaborating on the practical use of these ideas in light of the common restrictions that many academics encounter today while undertaking cooperative research. The book provides suggestions on how to improve cross disciplinary work in the future and share their own experiences conducting interdisciplinary studies. Students expectations about their own Internet computer skills and their capacity to complete online courses are explored in this book with research on online education self efficacy. The relevance of culture in the workplace is shown by the fact that several studies have examined the connection between business culture and factors like productivity and lifespan. As well as having a significant impact on a broad variety of organisational processes employees performance it has long been seen as a critical component in integrating the various business cultures within corporate group organisation. This book aims to chart the history of the electrochemical science from its inception as a

separate discipline to the present day *Proceedings of ASP-DAC/VLSI Design 2002* ,2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c *Eleventh International Conference on VLSI Design* VLSI Society of India,IEEE Circuits and Systems Society,1997 Areas covered in this work include physical design synthesis delay test and timing high level synthesis hardware software co design low power design verification VLSI synthesis testability enhancement asynchronous design diagnosis test and fault modelling and mixed signal design *Proceedings of the 2025 2nd International Conference on Electrical Engineering and Intelligent Control (EEIC 2025)* Ata Jahangir Moshayedi,2025-11-20 This is an open access book The organizing committee is honored to extend a heartfelt welcome to the 2nd International Conference on Electrical Engineering and Intelligent Control EEIC 2025 Building on the resounding success of its inaugural edition in Singapore 2024 as part of the Conference on Intelligent Collaboration CIC series this year s conference will convene in Auckland New Zealand reaffirming its role as a global nexus uniting leading researchers scholars and industry pioneers in electrical engineering and intelligent control Auckland s dynamic fusion of world class academia a thriving innovation ecosystem and a steadfast commitment to sustainability mirrors EEIC s vision for Collaborative Intelligence Ethical Innovation and Resilient Systems By hosting EEIC 2025 here we aim to harness the city s unique energy to address emerging challenges and drive technological progress with ethical foresight Under this guiding theme EEIC 2025 will catalyze cutting edge dialogue showcase transformative advancements and inspire collaborative solutions to shape the future of intelligent systems Through fostering synergy across disciplines we aspire to accelerate breakthroughs in both theoretical frameworks and real world applications ensuring resilient and equitable progress in these critical fields

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