



**1 b. Explain in detail with a neat figure the working of the internal architecture of the 8086 MP [08 marks]**

**Ans:**

### **Internal Architecture of 8086**

• The 8086 processor is divided into two functional units (Figure 1-2):

- 1) Bus Interface Unit (BIU)
- 2) Execution Unit (EU)

### **Bus Interface Unit**

• The BIU

- > sends out addresses
- > fetches instructions from memory
- > reads data from memory and
- > writes data to memory

• The functional parts of the BIU are:

#### **1) Instruction Queue**

- The Instruction Queue is of 6 bytes in length.
- This is used to send up the execution of programs by pre-fetching 6 instruction bytes in advance from memory.
- The BIU and EU works parallel. The BIU fetches the instruction bytes while the EU is executing an instruction.
- The process of pre-fetching the instruction in advance while EU is executing the current instruction is known as pipelining.

#### **2) Segment Register**

• The BIU contains four 16-bit segment register: CS, DS, SS and ES

- These registers are used to store the 16 bit starting address of the four memory segment.

#### **3) Instruction Pointer(IP) Register**

- It is used by the microprocessor to find the next sequential instruction in a program located within the code segment.

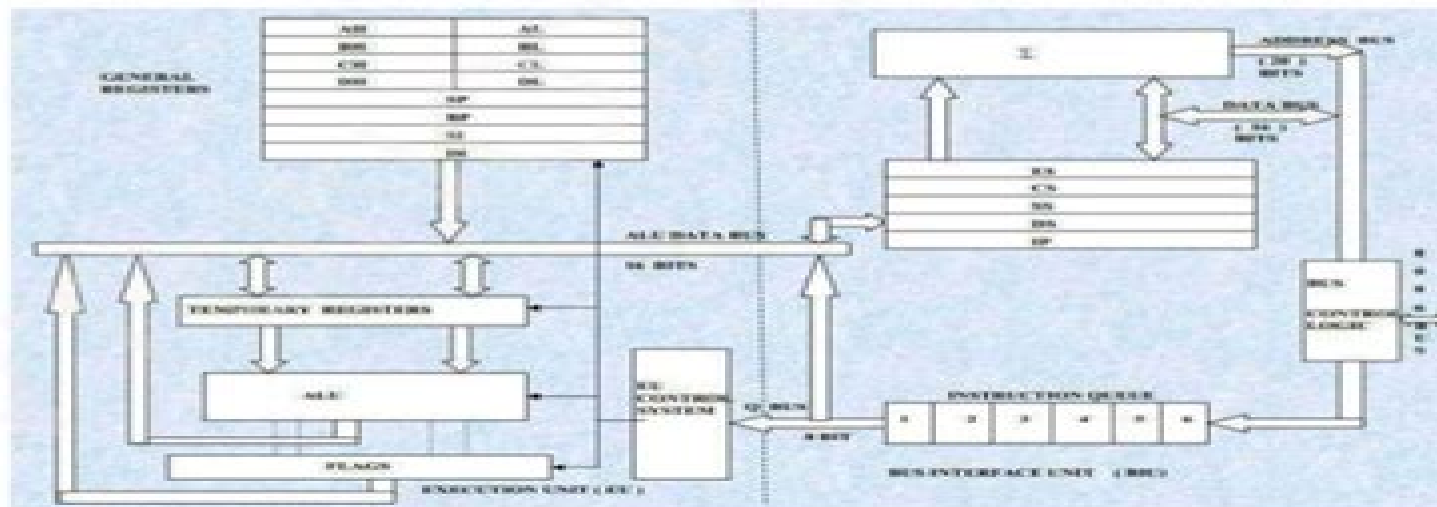


Figure 1-2: Internal Architecture of 8086

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