

Sample Papers

FINAL TERM EXAMINATION SPRING 2006 CS302 - DIGITAL LOGIC DESIGN (Session - 1)

Marks: 100
Time: 120min

Student ID/Login ID: _____
Student Name: _____
Center Name/Code: _____
Exam Date: _____ Saturday, August 19, 2006

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions.
2. Calculators are NOT allowed.
3. Do not ask any questions about the contents of this examination from anyone.
4. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
5. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.
6. Circuit Diagrams, Equations and Truth Tables should be clear. Write down all the steps in Subjective Questions. Marks will be deducted for missing steps.

****WARNING: Please note that Virtual University takes serious note of unfair means. Anyone found involved in cheating will get an 'F' grade in this course.**

Question	1	2	3	4	5	6	7	8	9	10	Total
Marks	11	12									
Question Marks											

Question No: 1 (Marks: 2) - Please choose one

What is the decimal value of the terminal count of a 4-bit binary counter?

- 10
- 12
- 15
- 16

Question No: 2 (Marks: 2) - Please choose one

The 1's complement of 10110111 is _____.

- 10110111
- 01001011
- 01101011
- 01001000

Question No: 3 (Marks: 2) - Please choose one

To serially shift a byte of data into a shift register, there must be?

- One clock pulse
- One load pulse
- Eight clock pulses
- One clock pulse for each 1 in the data.

Question No: 4 (Marks: 2) - Please choose one

What is the difference between a D latch and a D flip-flop?

- The D latch has a clock input.
- The D flip-flop has an enable input.
- The D latch is used for faster operation.
- The D flip-flop has a clock input.

Question No: 5 (Marks: 2) - Please choose one

For a positive edge triggered J-K flip-flop with both J and K HIGH, the outputs will _____ if the clock goes HIGH.

- toggle
- set
- reset
- not change

Question No: 6 (Marks: 12)

Draw the circuit diagram and truth table of the following equation.
 $F(x, y, z) = \sum (0, 2, 3, 5, 7)$

Question No: 7 (Marks: 10)

Draw the truth table of a Half-Adder. Draw the logical circuit diagram of a half-adder. Write Boolean expressions for all the output signals of half adder circuit.

Question No: 8 (Marks: 20)

Design a counter to produce the following sequence using J-K Flip-Flops.
1, 4, 3, 5, 7, 6, 2, 1

Question No: 9 (Marks: 12)

Draw the circuit diagram of the 2-input 4-bit Multiplexer. Also write down its function table?

Question No: 10 (Marks: 14)

a) For a gated D latch, determine the $\bar{Q}$ and $\bar{\bar{Q}}$ outputs for the inputs in figure. Show them in proper relation to the enable input. Assume $\bar{Q}$ starts LOW.



b) What is the difference between Flip-flop and latches?

Question No: 11 (Marks: 12)

a) What is the difference between SRAM and DRAM?
b) What is FIFO?
c) What is LIFO?

Question No: 12 (Marks: 10)

- a) What does sampling mean?
- b) Name any four performance characteristics of Digital-to-Analog Converters.
- c) Write name of Analog-to-Digital conversion methods

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J Ma



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