

**QUESTION PAPER CODE : 11343**  
**B.E./B.TECH. DEGREE EXAMINATION,**  
**NOVEMBER/DECEMBER 2012.**

**Sixth Semester**  
**Electronics and Communication Engineering**  
**EC 2354/EC64—VLSI DESIGN**  
**(Regulation 2008)**

**(Common to PTEC 2354—VLSI Design for B.E. (Part-Time)**  
**Fifth Semester-Electronics and Communication**  
**Engineering-Regulation 2009)**

**Time : Three hours**

**Maximum : 100 marks**

**Answer ALL questions.**

**PART A—(10 × 2 = 20 marks)**

1. Why the tunneling current is higher for NMOS transistors than PMOS transistors with silica gate?
2. What is the objective of layout rules?
3. Give the effect of supply voltage and temperature variations on the CMOS system performance.
4. What are the factors that cause static power dissipation in CMOS circuits?
5. State the reasons for the speed advantage of CVSL family.
6. Mention the qualities of an ideal sequencing method.
7. Distinguish testers and test fixtures.
8. What are the stages at which a chip can be tested?
9. Write the Verilog module for a 1-bit full adder.
10. Give an example for implicit continuous assignment.

**PART B—(5 × 16 = 80 marks)**

- 11.(a)(i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (10)

# Low Power Vlsi Design Question Paper

**Wenbin Ji**



## **Low Power Vlsi Design Question Paper:**

## Whispering the Strategies of Language: An Mental Quest through **Low Power Vlsi Design Question Paper**

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