

blue: signals to outside world

red: control signals latched by datain => CPU_S2
or
control signals driven by CPU_S1 for opcode
latching

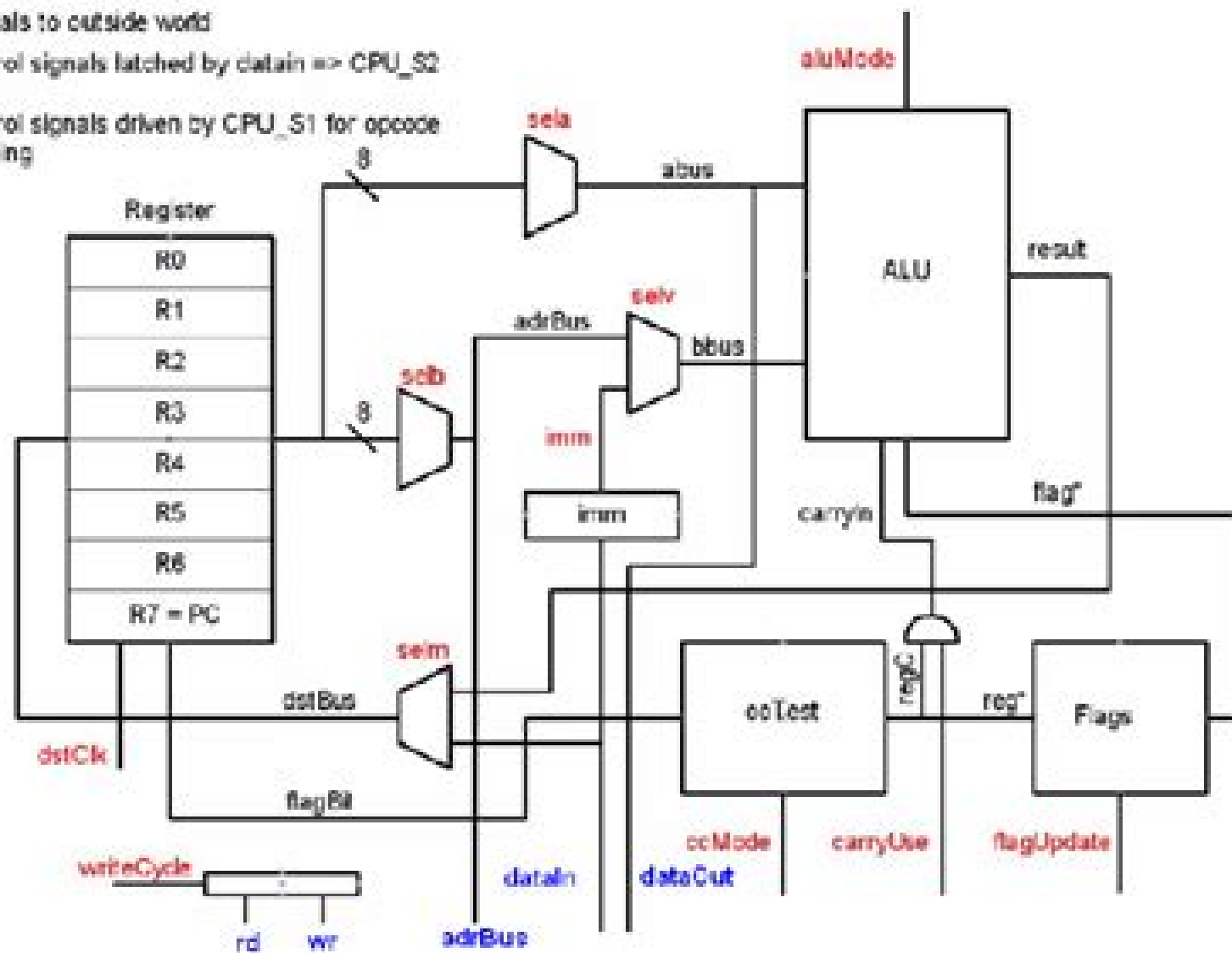


Figure 3. Data path for 64-bit RISC Processor [5]

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Smart Trends in Information Technology and Computer Communications A.V. Deshpande, Aynur Unal, Kalpdrum Passi, Dharm Singh, Malaya Nayak, Bharat Patel, Shafi Pathan, 2018-08-20 This book constitutes the refereed proceedings of the Second International Conference on Smart Trends in Information Technology and Computer Communications SmartCom 2017 held in Pune India in August 2017 The 38 revised papers presented were carefully reviewed and selected from 310 submissions The papers address issues on smart and secure systems smart and service computing smart data and IT innovations IEEE VLSI Test Symposium, 2000 **IEEE International Conference on Electronics, Circuits and Systems**, 2003 **18th IEEE VLSI Test Symposium**, 2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test compaction and design validation analog BIST and functional test and verification issues Also covered are STIL extension IDDQ test and on line testing and fault tolerance Lacks a subject index Annotation copyrighted by Book News Inc Portland OR **IEEE International Conference on Application-Specific Systems, Architectures and Processors** Lothar Thiele (Computer scientist), 1997 These conference papers on computer hardware and design and testing include coverage of miscellaneous applications arithmetic algorithms and architectures DSP architectures systolic algorithms and architectures rapid prototyping design methodologies and compilers **Rapid Prototyping of Application Specific Signal Processors** Mark A. Richards, Anthony J. Gadiant, Geoffrey A. Frank, 1997-02-28 Rapid Prototyping of Application Specific Signal Processors presents leading edge research that focuses on design methodology infrastructure support and scalable architectures developed by the 150 million dollar DARPA United States Department of Defense RASSP Program The contributions to this edited work include an introductory overview chapter that explains the origin concepts and status of this effort The RASSP Program is a multi year DARPA Tri Service initiative intended to dramatically improve the process by which complex digital systems particularly embedded signal processors are designed manufactured upgraded and supported This program was originally driven by military applications for signal processing The requirements of military applications for real

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