

Mohamed H. Abu-Rahma · Mohab Anis

Nanometer Variation-Tolerant SRAM

Circuits and Statistical Design for Yield

 Springer

Nanometer Variation Tolerant Sram

**Vikrant Bhateja, Jnyana Ranjan
Mohanty, Wendy Flores
Fuentes, Koushik Maharatna**



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Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-27 Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM shows an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages and higher variations make statistical simulation methodologies imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state-of-the-art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art variation tolerant SRAM circuit techniques. Discusses impact of device related process variations and how they affect circuit and system performance from a design point of view. Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques. **Nanometer**

Variation-Tolerant Sram, 2012-09-28

Low-Power Variation-Tolerant Design in Nanometer Silicon Swarup

Bhunia, Saibal Mukhopadhyay, 2010-11-10 Design considerations for low power operations and robustness with respect to variations typically impose contradictory requirements. Low power design techniques such as voltage scaling, dual threshold assignment and gate sizing can have large negative impact on parametric yield under process variations. This book focuses on circuit architectural design techniques for achieving low power operation under parameter variations. We consider both logic and memory design aspects and cover modeling and analysis as well as design methodology to achieve simultaneously low power and variation tolerance while minimizing design overhead. This book will discuss current industrial practices and emerging challenges at future technology nodes. *Data Science and Applications* Satyasai Jagannath Nanda, Rajendra

Prasad Yadav, Amir H. Gandomi, Mukesh Saraswat, 2024-02-24 This book gathers outstanding papers presented at the International Conference on Data Science and Applications ICDSA 2023 organized by Soft Computing Research Society SCRS and Malaviya National Institute of Technology Jaipur, India from 14 to 15 July 2023. The book is divided into four volumes and it covers theoretical and empirical developments in various areas of big data analytics, big data technologies, decision tree learning, wireless communication, wireless sensor networking, bioinformatics and systems, artificial neural networks, deep learning, genetic algorithms, data mining, fuzzy logic, optimization algorithms, image processing, computational intelligence in civil engineering and creative computing. **Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS**

Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs, GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density, performance and energy efficiency. This book delves into two primary areas within ultra-scaled technology nodes: 1. advancing SRAM bitcell scaling and 2. exploring

innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

Microelectronics, Electromagnetics and Telecommunications Jaume Anguera, Suresh Chandra Satapathy, Vikrant Bhateja, K.V.N. Sunitha, 2018-01-25 The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics Electromagnetics and Telecommunications ICMEET 2017 The conference was held during 09 10 September 2017 at Department of Electronics and Communication Engineering BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India The volume includes original and application based research papers on microelectronics electromagnetics telecommunications wireless communications signal speech video processing and embedded systems

Communication, Software and Networks Vikrant Bhateja, Jnyana Ranjan Mohanty, Wendy Flores Fuentes, Koushik Maharatna, 2022-10-27 This book highlights a collection of high quality peer reviewed research papers presented at the 7th International Conference on Information System Design and Intelligent Applications INDIA 2022 held at BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India from February 25 26 2022 It covers a wide range of topics in computer science and information technology from wireless networks social networks wireless sensor networks information and network security to web security Internet of Things bioinformatics geoinformatics and computer networks

VLSI Design and Test Brajesh Kumar Kaushik, Sudeb Dasgupta, Virendra Singh, 2017-12-21 This book

constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification

Energy Efficient and Reliable Embedded Nanoscale SRAM Design Bhupendra Singh Reniwal, Pooran Singh, Ambika Prasad Shah, Santosh Kumar Vishvakarma, 2023-11-29 This reference text covers a wide spectrum for designing robust embedded memory and peripheral circuitry It will serve as a useful text for senior undergraduate and graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering Discusses low power design methodologies for static random access memory SRAM Covers radiation hardened SRAM design for aerospace applications Focuses on various reliability issues that are faced by submicron technologies Exhibits more stable memory topologies Nanoscale technologies unveiled significant challenges to the design of energy efficient and reliable SRAMs This reference text investigates the impact of process variation leakage aging soft errors and related reliability issues in embedded memory and periphery circuitry The text adopts a unique way to explain the SRAM bitcell array design and analysis of its design parameters to meet the sub nano regime challenges for complementary metal oxide semiconductor devices It comprehensively covers low power design methodologies for SRAM exhibits more stable memory topologies and radiation hardened SRAM design for aerospace applications Every chapter includes a glossary highlights a question bank and problems The text will serve as a useful text for senior undergraduate students graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering Discussing comprehensive studies of variability induced failure mechanism in sense amplifiers and power delay and read yield trade offs this reference text will serve as a useful text for senior undergraduate graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering It covers the development of robust SRAMs well suited for low power multi core processors for wireless sensors node battery operated portable devices personal health care assistants and smart Internet of Things applications

Emerging Trends in Photonics, Signal Processing and Communication Engineering Govind R. Kadambi, Preetham B. Kumar, Vasile Palade, 2020-04-20 This volumes presents select papers presented during the International Conference on Photonics Communication and Signal Processing Technologies held in Bangalore from July 18th to 20th 2018 The research papers highlight analytical formulation solution simulation algorithm development experimental research and experimental investigations in the broad domains of photonics signal processing and communication technologies This volume will be of interest to researchers working in the field

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