Mohamed H. Abu-Rahma · Mohab Anis

# Nanometer Variation-Tolerant SRAM

Circuits and Statistical Design for Yield



# **Nanometer Variation Tolerant Sram**

S. Rajaram, N.B. Balamurugan, D. Gracia Nirmala Rani, Virendra Singh

#### **Nanometer Variation Tolerant Sram:**

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques Variation-Tolerant Sram ,2012-09-28 Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-27 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques Low-Power Variation-Tolerant Design in Nanometer Silicon Swarup Bhunia, Saibal Mukhopadhyay, 2010-11-10 Design considerations for low power operations and robustness with respect to variations typically impose contradictory requirements Low power design techniques such as voltage scaling dual threshold assignment and gate sizing can have large negative impact on parametric yield under process variations This book focuses on circuit architectural design techniques for achieving low power operation under parameter variations. We consider both logic and memory design aspects and cover modeling and analysis as well as design methodology to achieve simultaneously low power and variation tolerance while minimizing design overhead This book will discuss current industrial practices and emerging

challenges at future technology nodes <u>Data Science and Applications</u> Satyasai Jagannath Nanda, Rajendra Prasad Yaday, Amir H. Gandomi, Mukesh Saraswat, 2024-02-24 This book gathers outstanding papers presented at the International Conference on Data Science and Applications ICDSA 2023 organized by Soft Computing Research Society SCRS and Malaviya National Institute of Technology Jaipur India from 14 to 15 July 2023 The book is divided into four volumes and it covers theoretical and empirical developments in various areas of big data analytics big data technologies decision tree learning wireless communication wireless sensor networking bioinformatics and systems artificial neural networks deep learning genetic algorithms data mining fuzzy logic optimization algorithms image processing computational intelligence in civil engineering and creative computing Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes Microelectronics, Electromagnetics and Telecommunications Jaume Anguera, Suresh Chandra Satapathy, Vikrant Bhateja, K.V.N. Sunitha, 2018-01-25 The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics

Electromagnetics and Telecommunications ICMEET 2017 The conference was held during 09 10 September 2017 at Department of Electronics and Communication Engineering BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India The volume includes original and application based research papers on microelectronics electromagnetics telecommunications wireless communications signal speech video processing and embedded systems Software and Networks Vikrant Bhateja, Inyana Ranjan Mohanty, Wendy Flores Fuentes, Koushik Maharatna, 2022-10-27 This book highlights a collection of high quality peer reviewed research papers presented at the 7th International Conference on Information System Design and Intelligent Applications INDIA 2022 held at BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India from February 25 26 2022 It covers a wide range of topics in computer science and information technology from wireless networks social networks wireless sensor networks information and network security to web security Internet of Things bioinformatics geoinformatics and computer networks VLSI Design and Test Brajesh Kumar Kaushik, Sudeb Dasgupta, Virendra Singh, 2017-12-21 This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions. The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification Energy Efficient and Reliable Embedded Nanoscale SRAM Design Bhupendra Singh Reniwal, Pooran Singh, Ambika Prasad Shah, Santosh Kumar Vishvakarma, 2023-11-29 This reference text covers a wide spectrum for designing robust embedded memory and peripheral circuitry It will serve as a useful text for senior undergraduate and graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering Discusses low power design methodologies for static random access memory SRAM Covers radiation hardened SRAM design for aerospace applications Focuses on various reliability issues that are faced by submicron technologies Exhibits more stable memory topologies Nanoscale technologies unveiled significant challenges to the design of energy efficient and reliable SRAMs This reference text investigates the impact of process variation leakage aging soft errors and related reliability issues in embedded memory and periphery circuitry The text adopts a unique way to explain the SRAM bitcell array design and analysis of its design parameters to meet the sub nano regime challenges for complementary metal oxide semiconductor devices It comprehensively covers low power design methodologies for SRAM exhibits more stable memory topologies and radiation hardened SRAM design for aerospace applications Every chapter includes a glossary highlights a question bank and problems The text will serve as a useful text for senior undergraduate students graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering Discussing comprehensive studies of

variability induced failure mechanism in sense amplifiers and power delay and read yield trade offs this reference text will serve as a useful text for senior undergraduate graduate students and professionals in areas including electronics and communications engineering electrical engineering mechanical engineering and aerospace engineering It covers the development of robust SRAMs well suited for low power multi core processors for wireless sensors node battery operated portable devices personal health care assistants and smart Internet of Things applications **Emerging Trends in** Photonics, Signal Processing and Communication Engineering Govind R. Kadambi, Preetham B. Kumar, Vasile Palade, 2020-04-20 This volumes presents select papers presented during the International Conference on Photonics Communication and Signal Processing Technologies held in Bangalore from July 18th to 20th 2018 The research papers highlight analytical formulation solution simulation algorithm development experimental research and experimental investigations in the broad domains of photonics signal processing and communication technologies This volume will be of interest to researchers working in the field Proceedings of Sixth International Conference on Computer and Communication Technologies K. Reddy Madhavi, Nagaraj Ramrao, Kishore Kumar, K. Srujan Raju, Mathini Sellathurai, 2025-07-25 This book is a compilation of high quality scientific papers presented at the 6th International Conference on Computer Communication Technologies IC3T 2024 The book covers cutting edge technologies and applications of soft computing artificial intelligence and communication In addition a variety of further topics are discussed which include data mining machine intelligence fuzzy computing sensor networks signal and image processing human Near Threshold Computing Michael Hübner, Cristina Silvano, 2015-11-14 This computer interaction and web intelligence book explores near threshold computing NTC a design space using techniques to run digital chips processors near the lowest possible voltage Readers will be enabled with specific techniques to design chips that are extremely robust tolerating variability and resilient against errors Variability aware voltage and frequency allocation schemes will be presented that will provide performance guarantees when moving toward near threshold manycore chips Provides an introduction to near threshold computing enabling reader with a variety of tools to face the challenges of the power utilization wall Demonstrates how to design efficient voltage regulation so that each region of the chip can operate at the most efficient voltage and frequency point Investigates how performance guarantees can be ensured when moving towards NTC manycores through variability aware voltage and frequency allocation schemes <u>VLSI Design and Test</u> S. Rajaram, N.B. Balamurugan, D. Gracia Nirmala Rani, Virendra Singh, 2019-01-24 This book constitutes the refereed proceedings of the 22st International Symposium on VLSI Design and Test VDAT 2018 held in Madurai India in June 2018 The 39 full papers and 11 short papers presented together with 8 poster papers were carefully reviewed and selected from 231 submissions. The papers are organized in topical sections named digital design analog and mixed signal design hardware security micro bio fluidics VLSI testing analog circuits and devices network on chip memory quantum computing and NoC sensors and interfaces

**Microelectronics, Circuits and Systems** Abhijit Biswas, Aminul Islam, Rishu Chaujar, Olga Jaksic, 2023-06-26 This book covers the proceedings of the 8th International Conference on Microelectronics Circuits and Systems Micro2021 having design and developments of devices micro and nanotechnologies and electronic appliances This book includes the latest developments and emerging research topics in material sciences devices microelectronics circuits nanotechnology system design and testing simulation sensors photovoltaics optoelectronics and its different applications This book is of great attraction to researchers and professionals working in electronics microelectronics electrical and computer engineering

Hot Carrier Degradation in Semiconductor Devices Tibor Grasser,2014-10-29 This book provides readers with a variety of tools to address the challenges posed by hot carrier degradation one of today s most complicated reliability issues in semiconductor devices Coverage includes an explanation of carrier transport within devices and book keeping of how they acquire energy become hot interaction of an ensemble of colder and hotter carriers with defect precursors which eventually leads to the creation of a defect and a description of how these defects interact with the device degrading its performance

Micro and Nanoelectronics Devices, Circuits and Systems Trupti Ranjan Lenka, Durgamadhab Misra, Arindam Biswas, 2021-09-09 The book presents select proceedings of the International Conference on Micro and Nanoelectronics Devices Circuits and Systems MNDCS 2021 The volume includes cutting edge research papers in the emerging fields of micro and nanoelectronics devices circuits and systems from experts working in these fields over the last decade The book is a unique collection of chapters from different areas with a common theme and will be immensely useful to academic researchers and practitioners in the industry who work in this field **Design of Variation-tolerant Circuits for** Nanometer CMOS Technology Mohamed Hassan Abu-Rahma, 2008 Aggressive scaling of CMOS technology in sub 90nm nodes has created huge challenges Variations due to fundamental physical limits such as random dopants fluctuation RDF and line edge roughness LER are increasing significantly with technology scaling In addition manufacturing tolerances in process technology are not scaling at the same pace as transistor's channel length due to process control limitations e q sub wavelength lithography Therefore within die process variations worsen with successive technology generations These variations have a strong impact on the maximum clock frequency and leakage power for any digital circuit and can also result in functional yield losses in variation sensitive digital circuits such as SRAM Moreover in nanometer technologies digital circuits show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density It is therefore not surprising that the International Technology Roadmap for Semiconductors ITRS lists variability as one of the most challenging obstacles for IC design in nanometer regime To facilitate variation tolerant design we study the impact of random variations on the delay variability of a logic gate and derive simple and scalable statistical models to evaluate delay variations in the presence of within die variations This work provides new design insight and highlights the importance of

accounting for the effect of input slew on delay variations especially at lower supply voltages **Integrated Circuit and** System Design: Power and Timing Modeling, Optimization and Simulation José Monteiro, Rene van Leuken, 2010-02-18 This book constitutes the thoroughly refereed post conference proceedings of 19th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2009 featuring Integrated Circuit and System Design held in Delft The Netherlands during September 9 11 2009 The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability statistical timing circuit level techniques power management low power circuits technology system level techniques power timing optimization techniques self timed circuits low power circuit analysis optimization and low power design studies Communication, Networks and Computing Shekhar Verma, Ranjeet Singh Tomar, Brijesh Kumar Chaurasia, Vrijendra Singh, Jemal Abawajy, 2018-10-10 This book CCIS 839 constitutes the refereed proceedings of the First International Conference on Communication Networks and Computings CNC 2018 held in Gwalior India in March 2018 The 70 full papers were carefully reviewed and selected from 182 submissions. The papers are organized in topical sections on wired and wireless communication systems high dimensional data representation and processing networks and information security computing techniques for efficient networks design electronic circuits for communication system

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