

3. Show the complete timing diagram for the five-stage synchronous binary counter in the given figure. Verify that the waveforms of the Q outputs represent the correct binary number after each clock pulse.



4. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP or DOWN mode. Assume positive edge-triggering.
- 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0
5. For each of the cascaded counter configurations in the figure below, determine the frequency of the waveform at each point indicated by a circled number and then determine the overall modulus.



6. With general block diagrams, show how to obtain the following frequencies from a 10-MHz clock by using single flip-flops, modulus-5 counters, and decade counters:
- 5 MHz
  - 2.5 MHz
  - 2 MHz

# Et1220 Digital Fundamentals Final

**IM Harris**



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