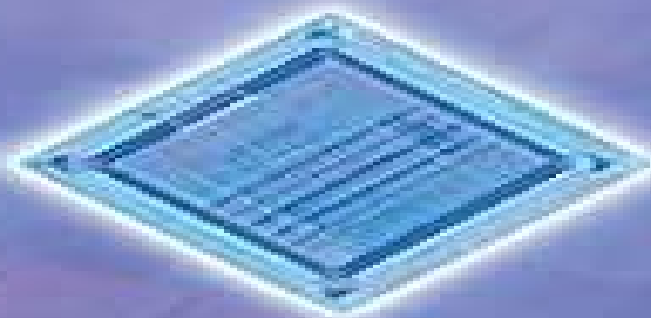


Low Power Methodology Manual

For System-on-Chip Design



Michael Keating David Flynn
Robert Aitken Alan Gibbons Kaijian Shi

 **Springer**

Low Power Methodology Manual

Kiat Seng Yeo, Kaixue Ma



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Low Power Methodology Manual David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, 2007-07-31 Tools alone aren't enough to reduce dynamic and leakage power in complex chip designs a well planned methodology is needed Following in the footsteps of the successful Reuse Methodology Manual RMM authors from ARM and Synopsys have written this Low Power Methodology Manual LPMM to describe such a low power methodology with a practical step by step approach Richard Goering Software Editor EE Times Excellent compendium of low power techniques and guidelines with balanced content spanning theory and practical implementation The LPMM is a very welcome addition to the field of low power SoC implementation that has for many years operated in a largely ad hoc fashion Sujeeth Joseph Chief Architect Semiconductor and Systems Solutions Unit Wipro Technologies The LPMM enables broader adoption of aggressive power management techniques based on extensive experience and silicon example with real data that every SOC designer can use to meet the difficulties faced in managing the power issues in deep submicron designs Anil Mankar Sr VP Worldwide Core Engineering and Chief Development Officer Conexant Systems Inc Managing power at 90nm and below introduces significant challenges to design flow The LPMM is a timely and immediately useful book that shows how combination of tools IP and methodology can be used together to address power management Nick Salter Head of Chip Integration CSR plc

Low Power Methodology Manual David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, 2007-12-19 This book provides a practical guide for engineers doing low power System on Chip SoC designs It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches In addition to providing a theoretical basis for these techniques the book addresses the practical issues of implementing them in today's designs with today's tools

Reuse Methodology Manual Pierre Bricaud, 2012-12-06 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re-examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant even as design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre-designed and pre-verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best

practices in the industry and to give a coherent integrated view of the design process Reuse Methodology Manual for System On A Chip Designs Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high quality SoC designs Reuse Methodology Manual for System-on-a-Chip Designs Pierre Bricaud, 2007-05-08 This revised and updated third edition outlines a set of best practices for creating reusable designs for use in an System on a Chip SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world Design and Modeling of Low Power VLSI Systems Sharma, Manoj, Gautam, Ruchi, Khan, Mohammad Ayoub, 2016-06-06 Very Large Scale Integration VLSI Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization Through a research based discussion of the technicalities involved in the VLSI hardware development process cycle this book is a useful resource for researchers engineers and graduate level students in computer science and engineering *Low Power Design Essentials* Jan Rabaey, 2009-04-21 Low Power Design Essentials contains all the topics of importance to the low power designer The book lays the foundation with background chapters entitled Advanced MOS Transistors and Their Models and Power Basics These chapters are followed by chapters on the design process including optimization architecture and algorithm level memory run time standby logic and standby memory Chapters on special topics are also included power management and modal design ultra low power and low power design methodology and flows The book concludes with a chapter on case studies as well as a chapter on Projection into the Future These chapters are all based on the extensive amount of teaching that the author has carried out both at universities and companies worldwide All chapters have been drawn up specifically for self study They aim however at different levels of understanding All the chapters start with elementary material but most also contain advanced material Ultra-Low Power Integrated Circuit Design Nianxiong Nick Tan, Dongmei Li, Zhihua Wang, 2013-10-23 This book describes the design of CMOS circuits for ultra low power consumption including analog radio frequency RF and digital signal processing circuits DSP The book addresses issues from circuit and system design to production design and applies the ultra low power circuits described to systems for digital hearing aids and capsule endoscope devices Provides a valuable introduction to ultra low power circuit design aimed at practicing design engineers Describes all key building blocks of ultra low power circuits from a systems perspective Applies circuits and systems described to real product examples such as hearing aids and capsule endoscopes Low-Power Wireless Communication Circuits and Systems Kiat Seng Yeo, Kaixue Ma, 2018-05-03 The increasing demand for extremely high data rate communications has urged researchers to develop new

communication systems Currently wireless transmission with more than one Giga bits per second Gbps data rates is becoming essential due to increased connectivity between different portable and smart devices To realize Gbps data rates millimeter wave MMW bands around 60 GHz is attractive due to the availability of large bandwidth of 9 GHz Recent research work in the Gbps data rates around 60 GHz band has focused on short range indoor applications such as uncompressed video transfer high speed file transfer between electronic devices and communication to and from kiosk Many of these applications are limited to 10 m or less because of the huge free space path loss and oxygen absorption for 60 GHz band MMW signal This book introduces new knowledge and novel circuit techniques to design low power MMW circuits and systems It also focuses on unlocking the potential applications of the 60 GHz band for high speed outdoor applications The innovative design application significantly improves and enables high data rate low cost communication links between two access points seamlessly The 60 GHz transceiver system on chip provides an alternative solution to upgrade existing networks without introducing any building renovation or external network laying works

An ASIC Low Power Primer Rakesh Chadha,J. Bhasker,2012-12-05 This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices Readers will benefit from the hands on approach which starts from the ground up explaining with basic examples what power is how it is measured and how it impacts on the design process of application specific integrated circuits ASICs The authors use both the Unified Power Format UPF and Common Power Format CPF to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent From analyzing system power consumption to techniques that can be employed in a low power design to a detailed description of two alternate standards for capturing the power directives at various phases of the design this book is filled with information that will give ASIC designers a competitive edge in low power design

Low Power Circuits for Emerging Applications in Communications, Computing, and Sensing Fei Yuan,2018-12-07 The book addresses the need to investigate new approaches to lower energy requirement in multiple application areas and serves as a guide into emerging circuit technologies It explores revolutionary device concepts sensors and associated circuits and architectures that will greatly extend the practical engineering limits of energy efficient computation The book responds to the need to develop disruptive new system architectures circuit microarchitectures and attendant device and interconnect technology aimed at achieving the highest level of computational energy efficiency for general purpose computing systems Features Discusses unique technologies and material only available in specialized journal and conferences Covers emerging applications areas such as ultra low power communications emerging bio electronics and operation in extreme environments Explores broad circuit operation ex analog RF memory and digital circuits Contains practical applications in the engineering field as well as graduate studies Written by international experts from both academia and industry

Languages, Design Methods, and Tools for Electronic System Design Daniel Große,Sara Vinco,Hiren Patel,2018-12-19 This book brings together

a selection of the best papers from the twentieth edition of the Forum on Specification and Design Languages Conference FDL which took place on September 18-20, 2017 in Verona, Italy. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware, software, embedded systems and mixed technology systems. Covers modeling and verification methodologies targeting digital and analog systems. Addresses firmware development and validation. Targets both functional and non-functional properties. Includes descriptions of methods for reliable system design. Verification Methodology Manual for Low Power Srikanth Jadcherla, 2009-01-01

ESL Models and their Application Brian Bailey, Grant Martin, 2009-12-15 This book arises from experience the authors have gained from years of work as industry practitioners in the field of Electronic System Level design. ESL is at the heart of all things related to Electronic Design Automation (EDA). The core issue is one of models: what are the models used for? What should the models contain and how should they be written and distributed? Issues such as interoperability and tool transportability become central factors that may decide which ones are successful and those that cannot get sufficient traction in the industry to survive. Through a set of real examples taken from recent industry experience, this book will distill the state of the art in terms of System Level Design models and provide practical guidance to readers that can be put into use. This book is an invaluable tool that will aid readers in their own designs, reduce risk in development projects, expand the scope of design projects and improve developmental processes and project planning. **Power-Aware Testing and Test Strategies for**

Low Power Devices Patrick Girard, Nicola Nicolici, Xiaoqing Wen, 2010-03-11 Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies such as dynamic voltage scaling, clock gating or power gating techniques are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test and power aware test is therefore increasingly becoming a major consideration during design for test and test preparation for low power devices. This book explores existing solutions for power aware test and design for test of conventional circuits and systems and surveys test strategies and EDA solutions for testing low power devices. *Integrated*

Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Jose L. Ayala, Braulio Garcia-Camara, Manuel Prieto, Martino Ruggiero, Gilles Sicard, 2011-09-15 This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design (PATMOS 2011) held in Madrid, Spain, in September 2011. The 34 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper features emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization. **Dual Mode Logic** Itamar

Levi, Alexander Fish, 2020-12-15 This book presents Dual Mode Logic DML a new design paradigm for digital integrated circuits DML logic gates can operate in two modes each optimized for a different metric Its on the fly switching between these operational modes at the gate block and system levels provide maximal E D optimization flexibility Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability All the facets of the DML methodology are covered starting from basic concepts through single gate optimization general module optimization design trade offs and new ways DML can be integrated into standard design flows using standard EDA tools DML logic is compatible with numerous applications but is particularly advantageous for ultra low power reliable high performance systems and advanced scaled technologies Written in language accessible to students and design engineers each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic Describes a novel promising alternative to conventional CMOS logic known as Dual Mode Logic DML with which a single gate can be operated selectively in two modes each optimized for a different metric e g energy consumption performance size Demonstrates several techniques at the architectural level which can result in high energy savings and improved system performance Focuses on the tradeoffs between power area and speed including optimizations at the transistor and gate level including alternatives to DML basic cells Illustrates DML efficiency for a variety of VLSI applications

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation José L. Ayala, Delong Shang, Alex

Yakovlev, 2013-01-03 This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design PATMOS 2012 held in Newcastle UK Spain in September 2012 The 25 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems including reconfigurable hardware such as FPGAs The technical program focus on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization

Introduction to VLSI Systems Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding

Adaptive Techniques for Dynamic Processor Optimization Alice Wang, Samuel Naffziger, 2008-07-23 The integrated circuit has evolved tremendously in recent years as Moore s Law has enabled exponentially more devices and functionality to be packed onto a single piece of silicon In some ways however these highly integrated circuits of which microprocessors are the flagship example have become victims of their own success Despite dramatic reductions in the switching energy of the transistors these reductions have kept pace neither with the increased

integration levels nor with the higher switching frequencies. In addition, the atomic dimensions being utilized by these highly integrated processors have given rise to much higher levels of random and systematic variation which undercut the gains from process scaling that would otherwise be realized. So these factors, the increasing impact of variation and the struggle to control power consumption, have given rise to a tremendous amount of innovation in the area of adaptive techniques for dynamic processor optimization. The fundamental premise behind adaptive processor design is the recognition that variations in manufacturing and environment cause a statically configured operating point to be far too inefficient. Inefficient designs waste power and performance and will quickly be surpassed by more adaptive designs just as it happens in the biological realm. Organisms must adapt to survive and a similar trend is seen with processors: those that are enabled to adapt to their environment will be far more competitive.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation Rene van Leuken, Gilles Sicard, 2011-01-16. This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble, France, in September 2010. The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows, circuit techniques, low power circuits, self-timed circuits, process variation, high level modeling of power-aware heterogeneous designs, in SystemC, AMS and minilogic.

Reviewing **Low Power Methodology Manual**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is actually astonishing. Within the pages of "**Low Power Methodology Manual**," an enthralling opus penned by a highly acclaimed wordsmith, readers set about an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve in to the book is central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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