

Synthesis of Hazard-free Customized CMOS Complex-gate Networks Under Multiple-Input Changes

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Abstract

This paper addresses the problem of realizing hazard-free single-output Boolean functions through a network of *customized CMOS gates* tailored to a given asynchronous controller specification. A customized CMOS gate network can either be a single CMOS gate or a multilevel network of CMOS gates. It is shown that hazard-free requirements for such networks are less restrictive than for simple gate networks. Analysis and efficient synthesis methods to generate such networks under a multiple-input change assumption (MIC) will be presented.

1 Introduction

This paper addresses the problem of realizing single-output Boolean functions through a network of *customized CMOS gates* for asynchronous controllers. A customized CMOS gate network can be either a single CMOS gate or a multilevel network of CMOS gates, where each CMOS gate is tailored to give the most efficient implementation for a given specification. This differs from the approach where one chooses standard gates from a library (such as AND-OR, MUX, AOI, etc.) to implement the required Boolean function in a hazard-free manner [7, 12, 5]. Techniques will be presented to synthesize such networks without hazards, under multiple-input change (MIC) transitions.

Customized CMOS gate implementations have been successfully used to design a large number of *burst-mode* asynchronous controllers [3, 13]. However, previous methods do not present systematic models and synthesis algorithms to take advantage of the particular hazard properties of these circuits. There are several reasons for considering customized CMOS complex-gate based circuits. As VLSI feature size decreases and wire delays become significant, customized CMOS complex-gates can provide more efficient controller implementations compared to standard-cell place and route tools. Also, the recent availability of better layout synthesis techniques that can automatically generate layouts for arbitrary transistor networks makes customized complex-gate based controllers a more viable alternative. Finally, we provide

methods to derive complex-gate networks which relax some of the synthesis constraints needed for hazard-free simple-gate implementations.

Currently, there are two main approaches to deriving hazard-free logic gate networks for asynchronous circuits. The first is a *function region* approach. In this method, one tries to find a hazard-free network for a single output Boolean function by taking into account the on-set and the off-set of the function, with respect to a specified set of multiple-input changes. The second approach deals with finding the *excitation regions* of the function. In this method, the regions of the Boolean space where the output is *enabled to change* are identified as “set” and “reset” functions. These functions are implemented and are used to control the switching of a state holding element such as a C-element or RS latch.

Various techniques for hazard-free logic minimization have been proposed for the function region approach. An exact hazard-free two-level logic minimization algorithm, based on a modified Quine-McCluskey method, is given in [7]. Hazard non-increasing transformations and algorithms for *multilevel* optimization of gate-level logic have been given in [4, 14]. A BDD-based method [5] which targets multilevel multiplexor-based networks has been developed. *Technology-mapping* techniques to perform hazard non-increasing mapping of two level AND-OR networks into complex gate networks from a standard cell library have been given in [12]. Other technology mapping techniques have implemented Boolean functions as single gate hazard-free CMOS complex gate circuits [13, 3]. However, no systematic procedure to derive such CMOS gates has been outlined, which includes precise hazard-free requirements for these gates.

For the class of methods that use the excitation regions, single CMOS complex-gate circuits, called Generalized C elements [6], have been used as target implementations. These techniques usually rely on the use of state holding elements on the output of the gate.

The contribution of this paper is to address the problem of deriving hazard-free customized CMOS realizations for asynchronous controllers under multiple-input changes, using the function region approach. This problem is encountered during the synthesis of burst-mode circuits [8, 15] and is a general problem in asynchronous synthesis. In particular, we present a style of CMOS gate design, called *SOP/SOP form*, that *reduces* the constraints in hazard-free synthesis of single CMOS complex gates. Second, we present a generalization of this technique to multilevel networks. This technique allows efficient solutions to a large class of asynchronous specifications. These techniques allow designers the flexibility to perform hazard-free mapping tailored to customized complex-gates, instead of being confined to a standard library.

In Section 2, we will introduce some basic terminology. Section 3 describes a technique to derive single CMOS complex gates. We will present techniques that address multilevel synthesis of such complex gate circuits in Section 4. Section 5 will provide conclusions and the open problems.

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