Nikhil Jayakumar Suganth Paul Rajesh Garg Kanupriya Gulati Sunil P. Khatri

Minimizing and Exploiting Leakage in VLSI Design



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Dr. M. Maheswaran, Mandadupu Anusha, Bandam Narendar, Modugu Rambabu

Minimizing And Exploiting Leakage In Vlsi Design:

Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar, Suganth Paul, Rajesh Garg, 2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of an IC However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs This book presents two techniques aimed at reducing leakage power in digital VLSI ICs The first technique reduces leakage through the selective use of high threshold voltage sleep transistors. The second technique reduces leakage by applying the optimal Reverse Body Bias RBB voltage This book also shows readers how to turn the leakage problem into an opportunity through the use of sub threshold logic Minimizing and Exploiting Leakage in **VLSI** Nikhil Jayakumar, 2010 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of VLSI circuits However due to process scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits This dissertation explores techniques to reduce leakage as well as techniques to exploit leakage currents through the use of sub threshold circuits This dissertation consists of two studies In the first study techniques to reduce leakage are presented These include a low leakage ASIC design methodology that uses high VT sleep transistors selectively a methodology that combines input vector control and circuit modification and a scheme to find the optimum reverse body bias voltage to minimize leakage As the minimum feature size of VLSI fabrication processes continues to shrink with each successive process generation along with the value of supply voltage and therefore the threshold voltage of the devices leakage currents increase exponentially Leakage currents are hence seen as a necessary evil in traditional VLSI design methodologies. We present an approach to turn this problem into an opportunity In the second study in this dissertation we attempt to exploit leakage currents to perform computation We use sub threshold digital circuits and come up with ways to get around some of the pitfalls associated with sub threshold circuit design These include a technique that uses body biasing adaptively to compensate for Process Voltage and Temperature PVT variations a design approach that uses asynchronous micro pipelined Network of Programmable Logic Arrays NPLAs to help improve the throughput of sub threshold designs and a method to find the optimum supply voltage that minimizes energy consumption in a circuit **Exploring the Intricacies of Digital and Analog VLSI Guha**, Koushik, Kandpal, Jyoti, Devi, Swagata, 2025-04-16 Advancements in Very Large Scale Integration VLSI technology are at the

heart of modern electronic innovation enabling the integration of millions of transistors onto a single chip This field is essential for developing efficient high performance systems that power everything from smartphones to advanced computing technologies By addressing both digital and analog VLSI design this topic explores the challenges and solutions involved in optimizing power signal integrity and functionality The impact of VLSI extends across industries driving technological progress and shaping the future of electronics in an increasingly interconnected world Exploring the Intricacies of Digital and Analog VLSI explores advanced techniques practical applications and emerging trends in both digital and analog VLSI It consolidates existing knowledge while introducing cutting edge methodologies and insights shaping the trajectory of future research endeavors in VLSI This book covers topics such as electrical engineering optimization techniques and computer science and is a useful resource for engineers computer scientists academicians and researchers **Ubiquitous** Computing Application and Wireless Sensor James J. (Jong Hyuk) Park, Yi Pan, Han-Chieh Chao, Gangman Yi, 2015-03-04 IT changes everyday s life especially in education and medicine The goal of ITME 2014 is to further explore the theoretical and practical issues of Ubiquitous Computing Application and Wireless Sensor Network It also aims to foster new ideas and collaboration between researchers and practitioners The organizing committee is soliciting unpublished papers for the main conference and its special tracks Transactions on High-Performance Embedded Architectures and Compilers III Per Stenström, 2011-02-23 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This third issue contains 14 papers carefully reviewed and selected out of numerous submissions and is divided into four sections The first section contains the top four papers from the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in G teborg Sweden in January 2008 The second section consists of four papers from the 8th MEDEA Workshop held in conjunction with PACT 2007 in Brasov Romania in September 2007 The third section contains two regular papers and the fourth section provides a snapshot from the First Workshop on Programmability Issues for Multicore Computers MULTIPROG held in conjunction with HiPEAC 2008 Dark Silicon and Future On-chip Systems, 2018-07-26 Dark Silicon and the Future of On chip Systems Volume 110 the latest release in the Advances in Computers series published since 1960 presents detailed coverage of innovations in computer hardware software theory design and applications with this release focusing on an Introduction to dark silicon and future processors a Revisiting of processor allocation and application mapping in future CMPs in the dark silicon era Multi objectivism in the dark silicon age Dark silicon aware resource management for many core systems Dynamic power

management for dark silicon multi core processors Topology specialization for networks on chip in the dark silicon era and Emerging SRAM based FPGA architectures Provides in depth surveys and tutorials on new computer technology Covers well known authors and researchers in the field Presents extensive bibliographies with most chapters Includes volumes that are devoted to single themes or subfields of computer science with this release focusing on Dark Silicon and Future On chip Transition of HPC Towards Exascale Computing Erik H. D'Hollander, Jack J. Dongarra, Ian Foster, Lucio Grandinetti, 2013-10-15 The US Europe Japan and China are racing to develop the next generation of supercomputers exascale machines capable of 10 to the 18th power calculations a second by 2020 But the barriers are daunting the challenge is to change the paradigm of high performance computing The 2012 biennial high performance workshop held in Cetraro Italy in June 2012 focused on the challenges facing the computing research community to reach exascale performance in the next decade This book presents papers from this workshop arranged into four major topics energy scalability new architectural concepts and programming of heterogeneous computing systems Chapter 1 introduces the status of present supercomputers which are still about two orders of magnitude separated from the exascale mark Chapter 2 examines energy demands a major limiting factor of today s fastest supercomputers the quantum leap in performance required for exascale computing will require a shift in architectures and technology In Chapter 3 scalable computer paradigms for dense linear algebra on massive heterogeneous systems are presented and Chapter 4 discusses architectural concepts Finally Chapter 5 addresses the programming of heterogeneous systems This book will be of interest to all those wishing to understand how the development of modern supercomputers is set to advance in the next decade **Advances in Computer Systems** Architecture Chris Jesshope, 2006-08-31 This book constitutes the refereed proceedings of the 11th Asia Pacific Computer Systems Architecture Conference ACSAC 2006 The book presents 60 revised full papers together with 3 invited lectures addressing such issues as processor and network design reconfigurable computing and operating systems and low level design issues in both hardware and systems Coverage includes large and significant computer based infrastructure projects the challenges of stricter budgets in power dissipation and more VLSI and Chip Design Dr. M. Maheswaran, Mandadupu Anusha, Bandam Narendar, Modugu Rambabu, 2024-05-23 VLSI and Chip Design exploration of Very Large Scale Integration VLSI technology and the intricacies of modern chip design It fundamental principles advanced methodologies and the latest innovations in circuit design fabrication and testing With a focus on digital and analog systems this integrates theoretical concepts with practical applications catering to both beginners and professionals It emphasizes design optimization power efficiency and scalability making it an essential resource for engineers researchers and students aspiring to excel in semiconductor technology and integrated circuit design <u>VLSI Design and Test</u> Brajesh Kumar Kaushik, Sudeb Dasgupta, Virendra Singh, 2017-12-21 This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions. The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification

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