

I. VERILOG INTRODUCTION

Verilog is a hardware description language (HDL) that describes the functionality of hardware design and the synthesis tool converts hardware descriptions into an actual design that has combinational and sequential elements. Verilog language is simpler than VHDL. Verilog is based on C language, whereas VHDL is based on Ada and Pascal languages. Latest Verilog standard: IEEE Standard 1364-2005.

Verilog is basically a structural and behavior language and defines four abstraction levels to implement modules. With respect to the external environment, the module is viewed as identical irrespective of abstraction levels. But internal module implementation differs based on abstraction as described below.

1. Gate level – The module implementation is similar to the gate-level design description in terms of logic gates and interconnections between them.
2. Dataflow level – The module implementation depends on data flow specification i.e. how data flows and processes in the design circuit.
3. Switch level – The module implementation requires switch level knowledge to implement a design in terms of storage nodes, switches. This is the lowest level of abstraction.
4. Behavior level – The module implementation is similar to C language programming that includes algorithmic level implementation without worrying about hardware implementation details.

Above abstraction levels are also commonly mentioned with modeling terminology. The design can be implemented with a combination of gate-level, data flow, and behavioral modeling. The commonly heard term RTL (Register Transfer Level) in digital design is used for a combination of data flow and behavior modeling.

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