

RISC-V Instruction Set Summary

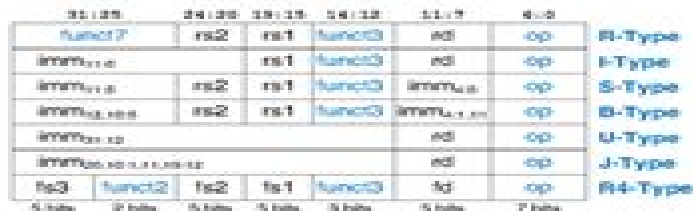


Figure B.1 RISC-V 32-bit instruction formats

- imm: signed immediate in $\text{imm}_{16\text{sb}}$
- uimm: 5-bit unsigned immediate in $\text{imm}_{5\text{ub}}$
- uopimm: 20 upper bits of a 32-bit immediate, in $\text{imm}_{20\text{ub}}$
- Address: memory address; $\text{rs1} + \text{SignExt}(\text{imm}_{16\text{sb}})$
- [Address]: data at memory location Address
- BTA: branch target address; $\text{PC} + \text{SignExt}(\text{imm}_{16\text{sb}}, 1'b0)$
- JTA: jump target address; $\text{PC} + \text{SignExt}(\text{imm}_{20\text{ub}}, 1'b0)$
- Label: text indicating instruction address
- SignExt: value sign-extended to 32 bits
- ZeroExt: value zero-extended to 32 bits
- CSR: control and status register

Table B.1 RV32I: RISC-V Integer Instructions

op	funct3	funct7	Type	Instruction	Description	Operation
0000011 (3)	000	—	I	lb rd, imm(rs1)	load byte	$\text{rd} = \text{SignExt}([\text{Address}]_{7:0})$
0000011 (3)	001	—	I	lh rd, imm(rs1)	load half	$\text{rd} = \text{SignExt}([\text{Address}]_{15:0})$
0000011 (3)	010	—	I	lw rd, imm(rs1)	load word	$\text{rd} = [\text{Address}]_{31:0}$
0000011 (3)	100	—	I	lbu rd, imm(rs1)	load byte unsigned	$\text{rd} = \text{ZeroExt}([\text{Address}]_{7:0})$
0000011 (3)	101	—	I	lhu rd, imm(rs1)	load half unsigned	$\text{rd} = \text{ZeroExt}([\text{Address}]_{15:0})$
0010011 (19)	000	—	I	addi rd, rs1, imm	add immediate	$\text{rd} = \text{rs1} + \text{SignExt}(\text{imm})$
0010011 (19)	001	0000000*	I	slli rd, rs1, uimm	shift left logical immediate	$\text{rd} = \text{rs1} \ll \text{uimm}$
0010011 (19)	010	—	I	slli rd, rs1, imm	set less than immediate	$\text{rd} = (\text{rs1} \ll \text{SignExt}(\text{imm}))$
0010011 (19)	011	—	I	slliu rd, rs1, imm	set less than imm, unsigned	$\text{rd} = (\text{rs1} \ll \text{SignExt}(\text{imm}))$
0010011 (19)	100	—	I	xori rd, rs1, imm	xor immediate	$\text{rd} = \text{rs1} \oplus \text{SignExt}(\text{imm})$
0010011 (19)	101	0000000*	I	srlr rd, rs1, uimm	shift right logical immediate	$\text{rd} = \text{rs1} \gg \text{uimm}$
0010011 (19)	101	0100000*	I	srair rd, rs1, uimm	shift right arithmetic imm.	$\text{rd} = \text{rs1} \ggg \text{uimm}$
0010011 (19)	110	—	I	ori rd, rs1, imm	or immediate	$\text{rd} = \text{rs1} \text{SignExt}(\text{imm})$
0010011 (19)	111	—	I	andir rd, rs1, imm	and immediate	$\text{rd} = \text{rs1} \& \text{SignExt}(\text{imm})$
0010111 (23)	—	—	U	auipc rd, uopimm	add upper immediate to PC	$\text{rd} = (\text{uopimm}, 12'b0) + \text{PC}$
0100011 (35)	000	—	S	sb rs2, imm(rs1)	store byte	$[\text{Address}]_{7:0} = \text{rs2}_{7:0}$
0100011 (35)	001	—	S	sh rs2, imm(rs1)	store half	$[\text{Address}]_{15:0} = \text{rs2}_{15:0}$
0100011 (35)	010	—	S	sw rs2, imm(rs1)	store word	$[\text{Address}]_{31:0} = \text{rs2}$
0110011 (51)	000	0000000	R	add rd, rs1, rs2	add	$\text{rd} = \text{rs1} + \text{rs2}$
0110011 (51)	000	0100000	R	sub rd, rs1, rs2	sub	$\text{rd} = \text{rs1} - \text{rs2}$
0110011 (51)	001	0000000	R	sll rd, rs1, rs2	shift left logical	$\text{rd} = \text{rs1} \ll \text{rs2}_{6:0}$
0110011 (51)	010	0000000	R	sll rd, rs1, rs2	set less than	$\text{rd} = (\text{rs1} \ll \text{rs2})$
0110011 (51)	011	0000000	R	sllui rd, rs1, rs2	set less than unsigned	$\text{rd} = (\text{rs1} \ll \text{rs2})$
0110011 (51)	100	0000000	R	xor rd, rs1, rs2	xor	$\text{rd} = \text{rs1} \oplus \text{rs2}$
0110011 (51)	101	0000000	R	srl rd, rs1, rs2	shift right logical	$\text{rd} = \text{rs1} \gg \text{rs2}_{6:0}$
0110011 (51)	101	0100000	R	sra rd, rs1, rs2	shift right arithmetic	$\text{rd} = \text{rs1} \ggg \text{rs2}_{6:0}$
0110011 (51)	110	0000000	R	or rd, rs1, rs2	or	$\text{rd} = \text{rs1} \text{rs2}$
0110011 (51)	111	0000000	R	and rd, rs1, rs2	and	$\text{rd} = \text{rs1} \& \text{rs2}$
0110111 (35)	—	—	U	lui rd, uopimm	load upper immediate	$\text{rd} = (\text{uopimm}, 12'b0)$
1100011 (99)	000	—	B	beq rs1, rs2, label	branch if =	if ($\text{rs1} == \text{rs2}$) $\text{PC} = \text{BTA}$
1100011 (99)	001	—	B	bne rs1, rs2, label	branch if ≠	if ($\text{rs1} \neq \text{rs2}$) $\text{PC} = \text{BTA}$
1100011 (99)	100	—	B	blt rs1, rs2, label	branch if <	if ($\text{rs1} < \text{rs2}$) $\text{PC} = \text{BTA}$
1100011 (99)	101	—	B	bge rs1, rs2, label	branch if ≥	if ($\text{rs1} \geq \text{rs2}$) $\text{PC} = \text{BTA}$
1100011 (99)	110	—	B	bltu rs1, rs2, label	branch if < unsigned	if ($\text{rs1} < \text{rs2}$) $\text{PC} = \text{BTA}$
1100011 (99)	111	—	B	bgeu rs1, rs2, label	branch if ≥ unsigned	if ($\text{rs1} \geq \text{rs2}$) $\text{PC} = \text{BTA}$
1101111 (103)	000	—	I	jalr rd, rs1, imm	jump and link register	$\text{PC} = \text{rs1} + \text{SignExt}(\text{imm})$, $\text{rd} = \text{PC} + 4$
1101111 (111)	—	—	J	jal rd, label	jump and link	$\text{PC} = \text{JTA}$, $\text{rd} = \text{PC} + 4$

*Encoded in $\text{instr}_{6:0}$, the upper seven bits of the immediate field

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