

Con. 3002-10.

(3 Hours)

AN-2512

[ Total Marks : 100

N.B. (1) Question No. 1 is compulsory.

(2) Attempt any four out of remaining six questions.

(3) Figures to the right indicate full marks.

1. (a) Compare Synchronous and Asynchronous Counter. 4  
 (b) Convert  $(BC-ACD)_{16}$  to Octal, Decimal, Binary. 4  
 (c) Prove that  $[ AB + C ( \overline{AB} + \overline{AC} ) ] = AB$ . 4  
 (d) A seven bit even parity hamming code is received as 1111101. What is correct data ? 4  
 (e) Perform  $13-22$  using  $2^s$  complement method and  $8-2$  using 9s complement method. 4
2. (a) Show that— 10  

$$[ (A+B) (A+B) ] + [ (CD + \overline{CD}) + (C \oplus D) ] = 1$$
  
 (b) Simplify and implement using Logic gates 10  

$$Y = ( \overline{A} + \overline{B} ) (B + C) + AB ( \overline{BC} )$$
3. (a) Minimize the following expressin using K-map and realize the circuit using gates 8  

$$= \sum m(0, 1, 3, 5, 7, 8, 9, 10, 11, 12, 14)$$
  
 (b) Simplify the following Boolean function by using Quine MC Clusky method : 12  

$$f(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13).$$
4. (a) Design a BCD to 7 segment (common anode) code converter. Realize the circuit using suitable gates. 12  
 (b) Design full subtractor using Logic gates. 8
5. (a) Convert D flip-flop in to T flip-flop. 10  
 (b) Design MOD-12 asynchronous ripple counter. 10
6. (a) What is shift register ? How a shift register can be modified to ring counter and twisted ring counter. 10  
 (b) Design MOD-5 synchronous counter using J-K flip-flop. 10
7. (a) What is programmable logic array (PLA) ? Explain with a neat diagram. What are advantages of PLDs ? 10  
 (b) What are salient features of TTL family ? Explain following features in relation to TTL family :— 10  
 (i) Totem Pole Output  
 (ii) Open Collector Output  
 (iii) Wired AND Connection.

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**D Keegan**



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