

QUESTION PAPER CODE : 11343
B.E./B.TECH. DEGREE EXAMINATION,
NOVEMBER/DECEMBER 2012.

Sixth Semester
Electronics and Communication Engineering
EC 2354/EC64—VLSI DESIGN
(Regulation 2008)

(Common to PTEC 2354—VLSI Design for B.E. (Part-Time)
Fifth Semester-Electronics and Communication
Engineering-Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A—(10 × 2 = 20 marks)

1. Why the tunneling current is higher for NMOS transistors than PMOS transistors with silica gate?
2. What is the objective of layout rules?
3. Give the effect of supply voltage and temperature variations on the CMOS system performance.
4. What are the factors that cause static power dissipation in CMOS circuits?
5. State the reasons for the speed advantage of CVSL family.
6. Mention the qualities of an ideal sequencing method.
7. Distinguish testers and test fixtures.
8. What are the stages at which a chip can be tested?
9. Write the Verilog module for a 1-bit full adder.
10. Give an example for implicit continuous assignment.

PART B—(5 × 16 = 80 marks)

- 11.(a)(i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (10)

Low Power Vlsi Design Question Paper

Judd E. Hollander



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Table of Contents Low Power Vlsi Design Question Paper

1. Understanding the eBook Low Power Vlsi Design Question Paper
 - The Rise of Digital Reading Low Power Vlsi Design Question Paper
 - Advantages of eBooks Over Traditional Books
2. Identifying Low Power Vlsi Design Question Paper
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Low Power Vlsi Design Question Paper
 - User-Friendly Interface
4. Exploring eBook Recommendations from Low Power Vlsi Design Question Paper
 - Personalized Recommendations
 - Low Power Vlsi Design Question Paper User Reviews and Ratings
 - Low Power Vlsi Design Question Paper and Bestseller Lists
5. Accessing Low Power Vlsi Design Question Paper Free and Paid eBooks
 - Low Power Vlsi Design Question Paper Public Domain eBooks
 - Low Power Vlsi Design Question Paper eBook Subscription Services
 - Low Power Vlsi Design Question Paper Budget-Friendly Options
6. Navigating Low Power Vlsi Design Question Paper eBook Formats

- ePub, PDF, MOBI, and More
- Low Power Vlsi Design Question Paper Compatibility with Devices
- Low Power Vlsi Design Question Paper Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Low Power Vlsi Design Question Paper
 - Highlighting and Note-Taking Low Power Vlsi Design Question Paper
 - Interactive Elements Low Power Vlsi Design Question Paper
- 8. Staying Engaged with Low Power Vlsi Design Question Paper
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Low Power Vlsi Design Question Paper
- 9. Balancing eBooks and Physical Books Low Power Vlsi Design Question Paper
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Low Power Vlsi Design Question Paper
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Low Power Vlsi Design Question Paper
 - Setting Reading Goals Low Power Vlsi Design Question Paper
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Low Power Vlsi Design Question Paper
 - Fact-Checking eBook Content of Low Power Vlsi Design Question Paper
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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