

Mnemonic	Instruction	Description	Addressing Mode	# of Bytes	# of Cycles
MOV	A, #Data	$A \leftarrow \text{Data}$	Immediate	2	1
	A, Rn	$A \leftarrow Rn$	Register	1	1
	A, Direct	$A \leftarrow (\text{Direct})$	Direct	2	1
	A, @Ri	$A \leftarrow @Ri$	Indirect	1	1
	Rn, #Data	$Rn \leftarrow \text{data}$	Immediate	2	1
	Rn, A	$Rn \leftarrow A$	Register	1	1
	Rn, Direct	$Rn \leftarrow (\text{Direct})$	Direct	2	2
	Direct, A	$(\text{Direct}) \leftarrow A$	Direct	2	1
	Direct, Rn	$(\text{Direct}) \leftarrow Rn$	Direct	2	2
	Direct1, Direct2	$(\text{Direct1}) \leftarrow (\text{Direct2})$	Direct	3	2
	Direct, @Ri	$(\text{Direct}) \leftarrow @Ri$	Indirect	2	2
	Direct, #Data	$(\text{Direct}) \leftarrow \#Data$	Direct	3	2
	@Ri, A	$@Ri \leftarrow A$	Indirect	1	1
	@Ri, Direct	$@Ri \leftarrow \text{Direct}$	Indirect	2	2
	@Ri, #Data	$@Ri \leftarrow \#Data$	Indirect	2	1
	DPTR, #Data16	$DPTR \leftarrow \#Data16$	Immediate	3	2
MOVC	A, @A+DPTR	$A \leftarrow \text{Code Pointed by } A+DPTR$	Indexed	1	2
	A, @A+PC	$A \leftarrow \text{Code Pointed by } A+PC$	Indexed	1	2
	A, @Ri	$A \leftarrow \text{Code Pointed by } Ri \text{ (8-bit Address)}$	Indirect	1	2
MOVX	A, @DPTR	$A \leftarrow \text{External Data Pointed by } DPTR$	Indirect	1	2
	@Ri, A	$@Ri \leftarrow A \text{ (External Data 8-bit Addr)}$	Indirect	1	2
	@DPTR, A	$@DPTR \leftarrow A \text{ (External Data 16-bit Addr)}$	Indirect	1	2
PUSH	Direct	Stack Pointer $SP \leftarrow (\text{Direct})$	Direct	2	2
POP	Direct	$(\text{Direct}) \leftarrow \text{Stack Pointer } SP$	Direct	2	2
XCH	Rn	Exchange ACC with Rn	Register	1	1
	Direct	Exchange ACC with Direct Byte	Direct	2	1
	@Ri	Exchange ACC with Indirect RAM	Indirect	1	1
XCHD	A, @Ri	Exchange ACC with Lower Order Indirect RAM	Indirect	1	1

# Instruction Set Summary 8051

**Hongru Du**



## **Instruction Set Summary 8051:**

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