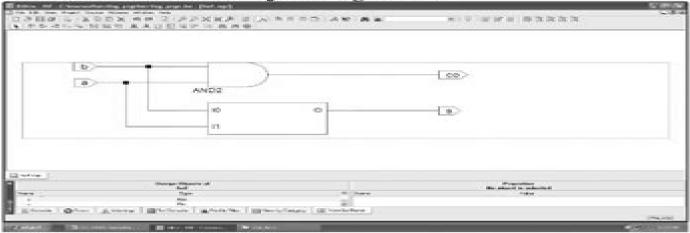


#### Synthesis:

#### Half Adder:





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# **Hdl And Verilog Vtu Lab Manual**

**Clemens Wendtner** 

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