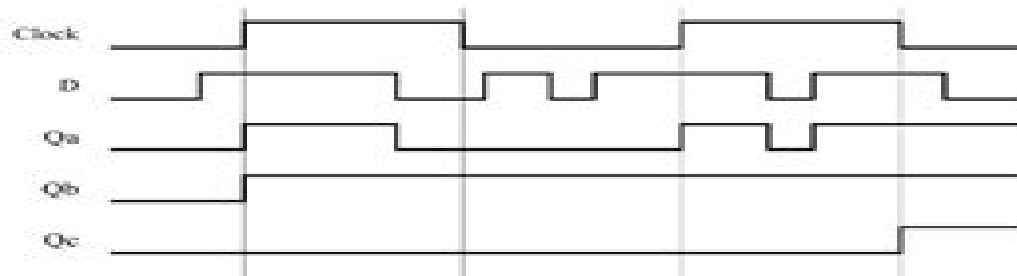


## Chapter 7

7.1.

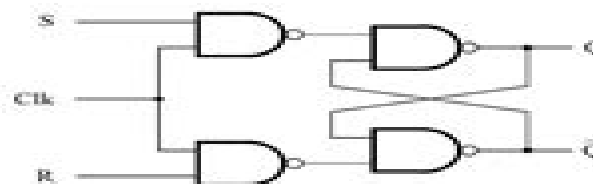


7.2. The circuit in Figure 7.3 can be modified to implement an SR latch by connecting  $S$  to the *Data* input and  $S + R$  to the *Load* input. Thus the value of  $S$  is loaded into the latch whenever either  $S$  or  $R$  is asserted. Care must be taken to ensure that the *Data* signal remains stable while the *Load* signal is asserted.

7.3.



7.4.



# Fundamental Of Digital Logic With Vhdl Design Solution Manual

**Yijin Wang**



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