

# Chapter 11

11.1. Label the wires in the circuit of Figure P11.1 as follows:

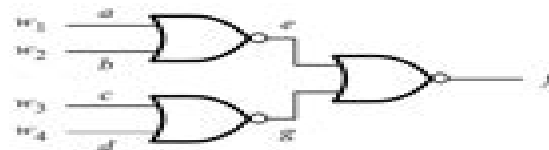


A complete fault table is

Test $w_1 w_2 w_3$	Fault detected									
	$a/0$	$a/1$	$b/0$	$b/1$	$c/0$	$c/1$	$d/0$	$d/1$	$f/0$	$f/1$
000								✓	✓	
001					✓		✓		✓	✓
010								✓	✓	
011		✓			✓		✓		✓	✓
100								✓	✓	
101				✓	✓		✓		✓	✓
110									✓	
111	✓		✓			✓			✓	

A minimal test set must include the tests  $w_1 w_2 w_3 = 011, 101$ , and  $111$ , which cover all faults except  $d/1$ . The latter fault can be detected by choosing one of  $000, 010$ , or  $100$ .

11.2. Label the wires in the circuit of Figure P11.2 as follows:



# Fundamentals Of Digital Logic With Verilog Design Solution Manual

**J Spring**



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