

QUESTION 1.

Mark Scheme
Cambridge IGCSE – May/June 2015



(b)

description of stage	seq. num.
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	3
the instruction is finally decoded and is then executed	7
<i>the PC (program counter) contains the address of the next instruction to be fetched</i>	(1)
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	4
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	2
the address part of the instruction is placed in the MAR (memory address register)	6
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	5*

The incrementation of the program counter can appear at any stage after 2. All other stages must be in the correct given order.

[6]

8 (a) hours: 18

minutes: 53

[2]

(b)

hours ("C")								:	minutes ("D")							
0	0	0	0	0	1	1	1	:	0	0	0	1	1	1	1	0

[2]

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G Thomas



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