



Verilog Manual Assertion

```
always_comb
  if (sel == 1'b1)
    out = a;
  else
    //pragma translate off
    if (sel == 1'b0)
      //pragma translate on
      out = b;
    //pragma translate off
    else // sel == 1'bX or 1'bZ
      begin
        out = 'x;
        $display(%m "assert:
          sel X or Z at time %d",
            $time);
      end
    //pragma translate on
```



```
always_comb
  if (sel) out = a;
  else out = b;
```



Microprocessor And Verilog And Manual

Annelies Wilder-Smith



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