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Jiyuan Zhang

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web the i 2c module contains an independent i 2c master logic and a i 2c slave logic which generates interrupts based on their events in the multi master systems the user software is simply partitioned into the master controller and the slave controller when the i 2c master logic is active the slave logic also remains active detecting the <a href="https://doi.org/10.2022/editable-10.2022/detable

web i2c master h this header contains i o definitions selection and timing clock speed settings used for the master i2c interface this file also includes prototypes of master i2c functions i2c master c this source file contains master i2c function implementations file

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub

modules spi serial peripheral interface i2c inter integrated circuit the inter integrated circuit commonly referred to as i2c is a synchronous two wire bidirectional serial communications bus

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web the i2c bus is a multi master serial data communication bus microcontrollers communicate in a master slave environment where the master devices initiate the communication and the devices are selected through addressing i2c operates with one or more master devices and one or more slave devices

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