

2-41.

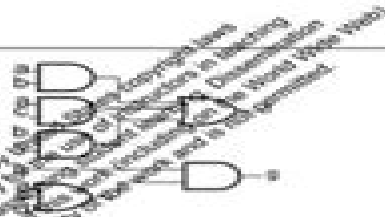
```

module circuit_4_51(X, F);
    input [2:0] X;
    output F;
    wire [0:4] T;
    nand
    nand
    g0(T[0], X[0], X[1]);
    g1(T[1], X[0], X[1]);
    g2(T[2], X[0], X[1], T[0]);
    g3(T[3], X[0], X[1], T[2]);
    g4(T[4], X[2], T[2]);
    g5(F, T[3], T[4]);
endmodule

```



2-42.



2-43.*

```

module circuit_4_53(X, Y, Z);
    input X, Y, Z;
    output F;
    assign F = (X & Z) | (Z & ~Y);
endmodule

```

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