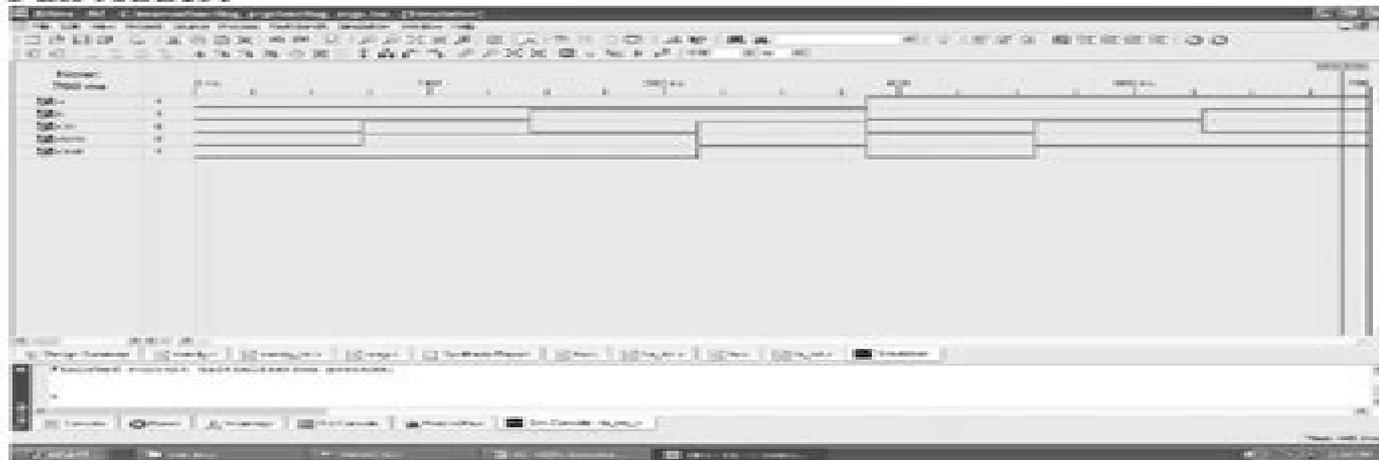


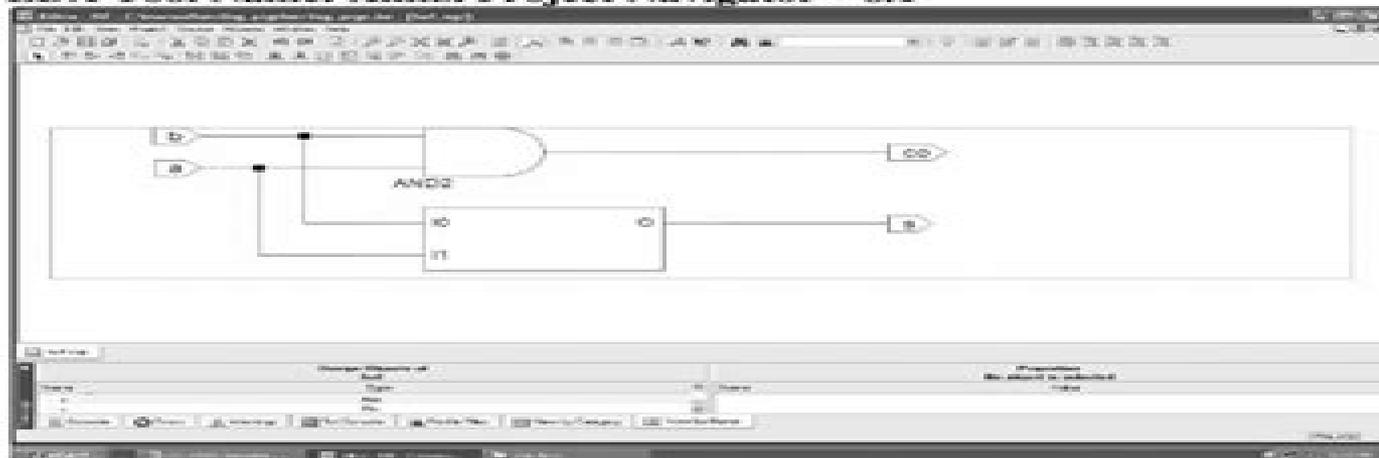
Full Adder:



Synthesis:

Half Adder:

EDA Tool Name: Xilinx Project Navigator – 8.1



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Hdl And Verilog Vtu Lab Manual

Minjie Lin



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