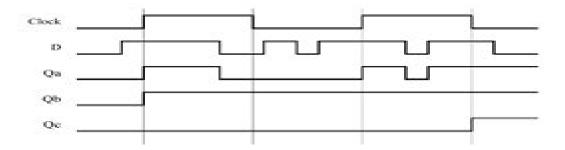
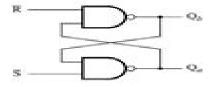
Chapter 7

7.1.



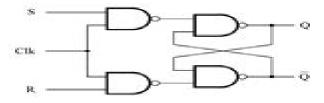
7.2. The circuit in Figure 7.3 can be modified to implement an SR latch by connecting S to the Data input and S + R to the Load input. Thus the value of S is loaded into the latch whenever either S or R is asserted. Care must be taken to ensure that the Data signal remains stable while the Load signal is asserted.

7.3.



SR	Qu	Q_{δ}	<u> </u>
11	30/1	170	(no change)
1 0	- 0	1.0	
0. 1	1.7	0	
0 0	1.0	1	

7.4.



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