Nikhil Jayakumar

Suganth Paul

Rajesh Garg

Kanupriya Gulati

Sunil P. Khatri

Minimizing and Exploiting Leakage in VLSI Design

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Minimizing And Exploiting Leakage In Vlsi Design

Anand J. Kulkarni,Suresh Chandra Satapathy,Tai Kang,Ali Husseinzadeh Kashan

Minimizing And Exploiting Leakage In Vlsi Design:

    Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar,Suganth Paul,Rajesh Garg,2010-04

    Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar,Suganth Paul,Rajesh Garg,2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of an IC However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs This book presents two techniques aimed at reducing leakage power in digital VLSI ICs The first technique reduces leakage through the selective use of high threshold voltage sleep transistors The second technique reduces leakage by applying the optimal Reverse Body Bias RBB voltage This book also shows readers how to turn the leakage problem into an opportunity through the use of sub threshold logic   *Minimizing and Exploiting Leakage in VLSI* Nikhil Jayakumar,2010 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of VLSI circuits However due to process scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits This dissertation explores techniques to reduce leakage as well as techniques to exploit leakage currents through the use of sub threshold circuits This dissertation consists of two studies In the first study techniques to reduce leakage are presented These include a low leakage ASIC design methodology that uses high VT sleep transistors selectively a methodology that combines input vector control and circuit modification and a scheme to find the optimum reverse body bias voltage to minimize leakage As the minimum feature size of VLSI fabrication processes continues to shrink with each successive process generation along with the value of supply voltage and therefore the threshold voltage of the devices leakage currents increase exponentially Leakage currents are hence seen as a necessary evil in traditional VLSI design methodologies We present an approach to turn this problem into an opportunity In the second study in this dissertation we attempt to exploit leakage currents to perform computation We use sub threshold digital circuits and come up with ways to get around some of the pitfalls associated with sub threshold circuit design These include a technique that uses body biasing adaptively to compensate for Process Voltage and Temperature PVT variations a design approach that uses asynchronous micro pipelined Network of Programmable Logic Arrays NPLAs to help improve the throughput of sub threshold designs and a method to find the optimum supply voltage that minimizes energy consumption in a circuit   **Exploring the Intricacies of Digital and Analog VLSI** Guha, Koushik,Kandpal, Jyoti,Devi,

Swagata,2025-04-16 Advancements in Very Large Scale Integration VLSI technology are at the heart of modern electronic innovation enabling the integration of millions of transistors onto a single chip This field is essential for developing efficient high performance systems that power everything from smartphones to advanced computing technologies By addressing both digital and analog VLSI design this topic explores the challenges and solutions involved in optimizing power signal integrity and functionality The impact of VLSI extends across industries driving technological progress and shaping the future of electronics in an increasingly interconnected world Exploring the Intricacies of Digital and Analog VLSI explores advanced techniques practical applications and emerging trends in both digital and analog VLSI It consolidates existing knowledge while introducing cutting edge methodologies and insights shaping the trajectory of future research endeavors in VLSI This book covers topics such as electrical engineering optimization techniques and computer science and is a useful resource for engineers computer scientists academicians and researchers **Ubiquitous Computing Application and Wireless Sensor** James J. (Jong Hyuk) Park,Yi Pan,Han-Chieh Chao,Gangman Yi,2015-03-04 IT changes everyday s life especially in education and medicine The goal of ITME 2014 is to further explore the theoretical and practical issues of Ubiquitous Computing Application and Wireless Sensor Network It also aims to foster new ideas and collaboration between researchers and practitioners The organizing committee is soliciting unpublished papers for the main conference and its special tracks **Languages and Compilers for Parallel Computing** Bill Pugh,Chau-Wen Tseng,2005-12-13 This book constitutes the thoroughly refereed post proceedings of the 15th International Workshop on Languages and Compilers for Parallel Processing LCPC 2002 held in College Park MD USA in July 2002 The 26 revised full papers presented were carefully selected during two rounds of reviewing and improvement from 32 submissions All current issues in parallel processing are addressed in particular memory constrained computation compiler optimization performance studies high level languages programming language consistency models dynamic parallelization parallelization of data mining algorithms parallelizing compilers garbage collection algorithms and evaluation of iterative compilation *Distributed Sensor Networks* S. Sitharama Iyengar,Richard R. Brooks,2022-06-01 The best selling Distributed Sensor Networks became the definitive guide to understanding this far reaching technology Preserving the excellence and accessibility of its predecessor Distributed Sensor Networks Second Edition once again provides all the fundamentals and applications in one complete self contained source Ideal as a tutorial for students or as research material for engineers the book gives readers up to date practical insight on all aspects of the field This two volume set this second edition has been revised and expanded with over 500 additional pages and more than 300 new illustrations This edition incorporates contributions from many veterans of the DARPA ISO SENSIT program as well as new material from distinguished researchers in the field It offers 13 fully revised chapters and 22 new chapters covering new perspectives on information fusion the latest technical developments and current sensor network applications Volume 1 Image and Sensor Signal Processing includes Distributed Sensing and Signal

Processing Information Fusion and Power Management Volume 2 Sensor Networking and Applications includes Sensor Deployment Adaptive Tasking Self Configuration System Control and Engineering Examples *Distributed Sensor Networks, Second Edition* S. Sitharama Iyengar,Richard R. Brooks,2012-09-24 The best selling Distributed Sensor Networks became the definitive guide to understanding this far reaching technology Preserving the excellence and accessibility of its predecessor Distributed Sensor Networks Second Edition once again provides all the fundamentals and applications in one complete self contained source Ideal as a tutorial for students or as research material for engineers the book gives readers up to date practical insight on all aspects of the field Revised and expanded this second edition incorporates contributions from many veterans of the DARPA ISO SENSIT program as well as new material from distinguished researchers in the field Image and Sensor Signal Processing focuses on software issues and the history and future of sensor networks The book also covers information fusion and power management Readers of this book may also be interested in Distributed Sensor Networks Second Edition Sensor Networking and Applications ISBN 9781439862872 *Emerging Technologies for Smart Cities* Prabin K. Bora,Sukumar Nandi,Shakuntala Laskar,2021-06-11 This book comprises the select proceedings of the International Conference on Emerging Global Trends in Engineering and Technology EGTET 2020 held in Guwahati India The chapters in this book focus on the latest cleaner greener and efficient technologies being developed for the implementation of smart cities across the world The broader topical sections include Smart Buildings Infrastructures and Disaster Management Smart Governance Technologies for Smart Cities and Wireless Connectivity for Smart Cities This book will cater to students researchers industry professionals and policy making bodies interested and involved in the planning and implementation of smart city projects *Proceedings of the 2nd International Conference on Data Engineering and Communication Technology* Anand J. Kulkarni,Suresh Chandra Satapathy,Tai Kang,Ali Husseinzadeh Kashan,2018-10-03 This book features research work presented at the 2nd International Conference on Data Engineering and Communication Technology ICDECT held on December 15 16 2017 at Symbiosis International University Pune Maharashtra India It discusses advanced multi disciplinary research into smart computing information systems and electronic systems focusing on innovation paradigms in system knowledge intelligence and sustainability that can be applied to provide feasible solutions to varied problems in society the environment and industry It also addresses the deployment of emerging computational and knowledge transfer approaches optimizing solutions in a variety of disciplines of computer science and electronics engineering **Power-efficient System Design** Preeti Ranjan Panda,B. V. N. Silpa,Aviral Shrivastava,Krishnaiah Gummidipudi,2010-07-23 The Information and communication technology ICT industry is said to account for 2% of the worldwide carbon emissions a fraction that continues to grow with the relentless push for more and more sophisticated computing equipment c munications infrastructure and mobile devices While computers evolved in the directionofhigherandhigherperformanceformostofthelatterhalfofthe20thc tury the late 1990 s and early 2000 ssaw a new

emergingfundamentalconcern that has begun to shape our day to day thinking in system design power dissipation As we elaborate in Chapter 1 a variety of factors colluded to raise power ef ciency as a rst class design concern in the designer s mind with profound consequences all over the eld semiconductor process design circuit design design automation tools system and application software all the way to large data centers Power ef cient System Design originated from a desire to capture and highlight the exciting developments in the rapidly evolving eld of power and energy op mization in electronic and computer based systems Tremendous progress has been made in the last two decades and the topic continues to be a fascinating research area To develop a clearer focus we have concentrated on the relatively higher level of design abstraction that is loosely called the system level In addition to the ext sive coverage of traditional power reduction targets such as CPU and memory the book is distinguished by detailed coverage of relatively modern power optimization ideas focussing on components such as compilers operating systems servers data centers and graphics processors **Proceedings of the ... ACM Great Lakes Symposium on VLSI.** ,2007 Adaptive Techniques for Dynamic Processor Optimization Alice Wang,Samuel Naffziger,2008-07-23 The integrated circuit has evolved tremendously in recent years as Moore s Law has enabled exponentially more devices and functionality to be packed onto a single piece of silicon In some ways however these highly integrated circuits of which microprocessors are the flagship example have become victims of their own success Despite dramatic reductions in the switching energy of the transistors these reductions have kept pace neither with the increased integration levels nor with the higher switching frequencies In addition the atomic dimensions being utilized by these highly integrated processors have given rise to much higher levels of random and systematic variation which undercut the gains from process scaling that would otherwise be realized So these factors the increasing impact of variation and the struggle to control power consumption have given rise to a tremendous amount of innovation in the area of adaptive techniques for dynamic processor optimization The fundamental premise behind adaptive processor design is the recognition that variations in manufacturing and environment cause a statically configured operating point to be far too inefficient Inefficient designs waste power and performance and will quickly be surpassed by more adaptive designs just as it happens in the biological realm Organisms must adapt to survive and a similar trend is seen with processors those that are enabled to adapt to their environment will be far more competitive **Robust SRAM Designs and Analysis** Jawar Singh,Saraju P. Mohanty,Dhiraj K. Pradhan,2012-08-01 This book provides a guide to Static Random Access Memory SRAM bitcell design and analysis to meet the nano regime challenges for CMOS devices and emerging devices such as Tunnel FETs Since process variability is an ongoing challenge in large memory arrays this book highlights the most popular SRAM bitcell topologies benchmark circuits that mitigate variability along with exhaustive analysis Experimental simulation setups are also included which cover nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Emphasis is placed throughout the book on the various trade offs for achieving a best SRAM bitcell design Provides a complete and

concise introduction to SRAM bitcell design and analysis Offers techniques to face nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Includes simulation set ups for extracting different design metrics for CMOS technology and emerging devices Emphasizes different trade offs for achieving the best possible SRAM bitcell design   Transition of HPC Towards Exascale Computing E.H. D'Hollander,2013-10-22 The US Europe Japan and China are racing to develop the next generation of supercomputers exascale machines capable of 10 to the 18th power calculations a second by 2020 But the barriers are daunting the challenge is to change the paradigm of high performance computing The 2012 biennial high performance workshop held in Cetraro Italy in June 2012 focused on the challenges facing the computing research community to reach exascale performance in the next decade This book presents papers from this workshop arranged into four major topics energy scalability new architectural concepts and programming of heterogeneous computing systems Chapter 1 introduces the status of present supercomputers which are still about two orders of magnitude separated from the exascale mark Chapter 2 examines energy demands a major limiting factor of today s fastest supercomputers the quantum leap in performance required for exascale computing will require a shift in architectures and technology In Chapter 3 scalable computer paradigms for dense linear algebra on massive heterogeneous systems are presented and Chapter 4 discusses architectural concepts Finally Chapter 5 addresses the programming of heterogeneous systems This book will be of interest to all those wishing to understand how the development of modern supercomputers is set to advance in the next decade   **CASES ...** ,2006   **Heterogeneous Computing** Mohamed Zahran,2019-05-29 If you look around you will find that all computer systems from your portable devices to the strongest supercomputers are heterogeneous in nature The most obvious heterogeneity is the existence of computing nodes of different capabilities e g multicore GPUs FPGAs But there are also other heterogeneity factors that exist in computing systems like the memory system components interconnection etc The main reason for these different types of heterogeneity is to have good performance with power efficiency Heterogeneous computing results in both challenges and opportunities This book discusses both It shows that we need to deal with these challenges at all levels of the computing stack from algorithms all the way to process technology We discuss the topic of heterogeneous computing from different angles hardware challenges current hardware state of the art software issues how to make the best use of the current heterogeneous systems and what lies ahead The aim of this book is to introduce the big picture of heterogeneous computing Whether you are a hardware designer or a software developer you need to know how the pieces of the puzzle fit together The main goal is to bring researchers and engineers to the forefront of the research frontier in the new era that started a few years ago and is expected to continue for decades We believe that academics researchers practitioners and students will benefit from this book and will be prepared to tackle the big wave of heterogeneous computing that is here to stay   *Nano-CMOS Circuit and Physical Design* Ban Wong,Anurag Mittal,Yu Cao,Greg W. Starr,2005-04-08 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit

and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation   The VLSI Handbook Wai-Kai Chen,2018-10-03 For the new millenium Wai Kai Chen introduced a monumental reference for the design analysis and prediction of VLSI circuits The VLSI Handbook Still a valuable tool for dealing with the most dynamic field in engineering this second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts models and equations Written by a stellar international panel of expert contributors this handbook is a reliable comprehensive resource for real answers to practical problems It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus WHAT S IN THE SECOND EDITION Sections on Low power electronics and design VLSI signal processing Chapters on CMOS fabrication Content addressable memory Compound semiconductor RF circuits High speed circuit design principles SiGe HBT technology Bipolar junction transistor amplifiers Performance modeling and analysis using SystemC Design languages expanded from two chapters to twelve Testing of digital systems Structured for convenient navigation and loaded with practical solutions The VLSI Handbook Second Edition remains the first choice for answers to the problems and challenges faced daily in engineering practice   Dual Mode Logic Itamar Levi,Alexander Fish,2020-12-15 This book presents Dual Mode Logic DML a new design paradigm for digital integrated circuits DML logic gates can operate in two modes each optimized for a different metric Its on the fly switching between these operational modes at the gate block and system levels provide maximal E D optimization flexibility Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability All the facets of the DML methodology are covered starting from basic concepts through single gate optimization general module optimization design trade offs and new ways DML can be integrated into standard design flows using standard EDA tools DML logic is compatible with numerous applications but is particularly advantageous for ultra low power reliable high performance systems and advanced scaled technologies Written in language accessible to students and design engineers each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic Describes a novel promising alternative to conventional CMOS logic known as Dual Mode Logic DML with which a single gate can be operated selectively in two modes each optimized for a different metric e g energy consumption performance size Demonstrates several techniques at the architectural level which can result in high energy savings and improved system performance Focuses on the tradeoffs between power area and speed including optimizations at the transistor and gate level including alternatives to DML basic cells Illustrates DML efficiency for a variety of VLSI applications

Unveiling the Magic of Words: A Report on "**Minimizing And Exploiting Leakage In Vlsi Design**"

In a world defined by information and interconnectivity, the enchanting power of words has acquired unparalleled significance. Their capability to kindle emotions, provoke contemplation, and ignite transformative change is really awe-inspiring. Enter the realm of "**Minimizing And Exploiting Leakage In Vlsi Design**," a mesmerizing literary masterpiece penned with a distinguished author, guiding readers on a profound journey to unravel the secrets and potential hidden within every word. In this critique, we shall delve to the book is central themes, examine its distinctive writing style, and assess its profound effect on the souls of its readers.

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