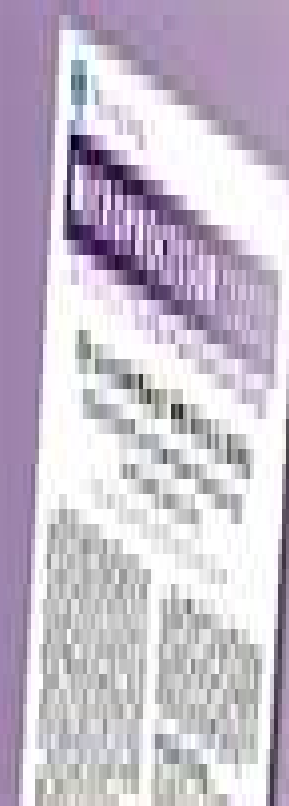


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Embedded Processor Design Challenges Ed F. Deprettere, Stamatis Vassiliadis, 2003-07-31 This textbook is intended to give an introduction to and an overview of state of the art techniques in the design of complex embedded systems. The book title is SAMOS for two major reasons. First it tries to focus on the actual distinct yet important problems of System Level design of embedded systems including mapping techniques and synthesis Architectural design Modeling issues such as specification languages formal models and finally Simulation. The second reason is that the volume includes a number of papers presented at a workshop with the same name on the Island of Samos Greece in July 2001. In order to receive international attention a number of reputed researchers were invited to this workshop to present their current work. Participation was by invitation only. For the volume presented here a number of additional papers were selected based on a call for papers. All contributions were refereed. This volume presents a selection of 18 of the refereed papers including 2 invited papers. The textbook is organized according to four topics. The first is A System Level Design and Simulation. In this section we present a collection of papers that give an overview of the challenging goal to design and explore alternatives of embedded system implementations at the system level. One paper gives an overview of models and tools used in system level design. The other papers present new models to describe applications provide models for refinement and design space exploration and for tradeoff analysis between cost and executability of an implementation. *Fast and Accurate Finite-Element Multigrid Solvers for PDE Simulations on GPU Clusters* Dominik GÖddeke, 2011 This dissertation demonstrates that graphics processors GPUs as representatives of emerging many core architectures are very well suited for the fast and accurate solution of large sparse linear systems of equations using parallel multigrid methods on heterogeneous compute clusters. Such systems arise for instance in the discretisation of elliptic partial differential equations with finite elements. Fine granular parallelisation techniques and methods to ensure accuracy are developed that enable at least one order of magnitude speedup over highly tuned conventional CPU implementations without sacrificing neither accuracy nor functionality. *Embedded Systems Handbook* Richard Zurawski, 2005-08-16 Embedded systems are nearly ubiquitous and books on individual topics or components of embedded systems are equally abundant. Unfortunately for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink. Until now The Embedded Systems Handbook is an oasis of information offering a mix of basic and advanced information. **Computerworld**, 2000-06-05 For more than 40 years Computerworld has been the leading source of technology news and information for IT influencers worldwide. Computerworld's award winning Web site Computerworld.com twice monthly publication focused conference series and custom research form the hub of the world's largest global IT media network. **Designing SOC's with Configured Cores** Steve Leibson, 2006-08-15 Microprocessor cores used for SOC design are the direct descendants of Intel's original 4004 microprocessor. Just as packaged microprocessor ICs vary widely in their attributes so do microprocessors packaged as IP cores. However SOC designers still

compare and select processor cores the way they previously compared and selected packaged microprocessor ICs The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades This assumption is no longer valid Processor cores for SOC designs can be far more plastic than microprocessor ICs for board level system designs Shaping these cores for specific applications produces much better processor efficiency and much lower system clock rates Together Tensilica's Xtensa and Diamond processor cores constitute a family of software compatible microprocessors covering an extremely wide performance range from simple control processors to DSPs to 3 way superscalar processors Yet all of these processors use the same software development tools so that programmers familiar with one processor in the family can easily switch to another This book emphasizes a processor centric MPSOC multiple processor SOC design style shaped by the realities of the 21st century and nanometer silicon It advocates the assignment of tasks to firmware controlled processors whenever possible to maximize SOC flexibility cut power dissipation reduce the size and number of hand built logic blocks shrink the associated verification effort and minimize the overall design risk An essential no nonsense guide to the design of 21st century mega gate SOC's using nanometer silicon Discusses today's key issues affecting SOC design based on author's decades of personal experience in developing large digital systems as a design engineer while working at Hewlett Packard's Desktop Computer Division and at EDA workstation pioneer Cadnetix and covering such topics as an award winning technology journalist and editor in chief for EDN magazine and the Microprocessor Report Explores conventionally accepted boundaries and perceived limits of processor based system design and then explodes these artificial constraints through a fresh outlook on and discussion of the special abilities of processor cores designed specifically for SOC design Thorough exploration of the evolution of processors and processor cores used for ASIC and SOC design with a look at where the industry has come from and where it's going Easy to understand explanations of the capabilities of configurable and extensible processor cores through a detailed examination of Tensilica's configurable extensible Xtensa processor core and six pre configured Diamond cores The most comprehensive assessment available of the practical aspects of configuring and using multiple processor cores to achieve very difficult and ambitious SOC price performance and power design goals

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