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Low Power Networks-on-Chip

Low Power Networks On Chip

**Konstantinos Tatas, Kostas
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Low Power Networks On Chip:

Low Power Networks-on-Chip Cristina Silvano, Marcello Lajolo, Gianluca Palermo, 2010-09-24 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures

Low Power Networks-on-Chip Cristina Silvano, Marcello Lajolo, Gianluca Palermo, 2010-10-06 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures

Networks on Chips Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs Networks-on-Chips Fayez Gebali, Haytham

Elmiligi, Mohamed Watheq El-Kharashi, 2011-06-03 The implementation of networks on chip NoC technology in VLSI integration presents a variety of unique challenges To deal with specific design solutions and research hurdles related to intra chip data exchange engineers are challenged to invoke a wide range of disciplines and specializations while maintaining a focused approach Leading Researchers Present Cutting Edge Designs Tools Networks on Chips Theory and Practice facilitates this process detailing the NoC paradigm and its benefits in separating IP design and functionality from chip communication requirements and interfacing It starts with an analysis of 3 D NoC architectures and progresses to a discussion of NoC resource allocation processor traffic modeling and formal verification with an examination of protocols at different layers of abstraction An exploration of design methodologies CAD tool development and system testing as well as communication protocol the text highlights important emerging research issues such as Resource Allocation for Quality of Service QoS on chip communication Testing verification and network design methodologies Architectures for interconnection real time monitoring and security requirements Networks on Chip Protocols Presents a flexible MPSoC platform to easily implement multimedia applications and evaluate future video encoding standards This useful guide tackles power and energy

issues in NoC based designs addressing the power constraints that currently limit the embedding of more processing elements on a single chip It covers traffic modeling and discusses the details of traffic generators Using unique case studies and examples it covers theoretical and practical issues guiding readers through every phase of system design *Analysis and Design of Networks-on-Chip Under High Process Variation* Rabab Ezz-Eldin, Magdy Ali El-Moursy, Hesham F. A. Hamed, 2015-12-16 This book describes in detail the impact of process variations on Network on Chip NoC performance The authors evaluate various NoC topologies under high process variation and explain the design of efficient NoCs with advanced technologies The discussion includes variation in logic and interconnect in order to evaluate the delay and throughput variation with different NoC topologies The authors describe an asynchronous router as a robust design to mitigate the impact of process variation in NoCs and the performance of different routing algorithms is determined with without process variation for various traffic patterns Additionally a novel Process variation Delay and Congestion aware Routing algorithm PDCR is described for asynchronous NoC design which outperforms different adaptive routing algorithms in the average delay and saturation throughput for various traffic patterns **Network-on-Chip** Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip

The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

Low-Power NoC for High-Performance SoC Design Hoi-Jun Yoo,Kangmin Lee,Jun Kyong Kim,2018-10-08 Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation Low Power NoC for High Performance SoC Design provides practical knowledge and real examples of how to use network on chip NoC in the design of system on chip SoC It discusses many architectural and theoretical studies on NoCs including design methodology topology exploration quality of service guarantee low power design and implementation trials The Steps to Implement NoC The book covers the full spectrum of the subject from theory to actual chip design using NoC Employing the Unified Modeling Language UML throughout it presents complicated concepts such as models of computation and communication computation partitioning in a manner accessible to laypeople The authors provide guidelines on how to simplify complex networking theory to design a working chip In addition they explore the novel NoC techniques and implementations of the Basic On Chip Network BONE project Examples of real time decisions circuit level design systems and chips give the material a real world context Low Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design this book shows how to build the complicated interconnections on SoC while keeping a low power consumption

Bio-Inspired Fault-Tolerant Algorithms for Network-on-Chip Muhammad Athar Javed Sethi,2020-03-17 Network on Chip NoC addresses the communication requirement of different nodes on System on Chip The bio inspired algorithms improve the bandwidth utilization maximize the throughput and reduce the end to end latency and inter flit arrival time This book exclusively presents in depth information regarding bio inspired algorithms solving real world problems focussing on fault tolerant algorithms inspired by the biological brain and implemented on NoC It further documents the bio inspired algorithms in general and more specifically in the design of NoC It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters Key Features Covers bio inspired solutions pertaining to Network on Chip NoC design solving real world examples Includes bio inspired NoC fault tolerant algorithms with detail coding examples Lists fault tolerant algorithms with detailed examples Reviews basic concepts of NoC Discusses NoC architectures developed to date

Designing 2D and 3D Network-on-Chip Architectures Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Large Scale Network-Centric Distributed Systems Hamid Sarbazi-Azad,Albert Y. Zomaya,2013-10-10 A highly accessible reference offering a broad range of topics and insights on

large scale network centric distributed systems Evolving from the fields of high performance computing and networking large scale network centric distributed systems continues to grow as one of the most important topics in computing and communication and many interdisciplinary areas Dealing with both wired and wireless networks this book focuses on the design and performance issues of such systems Large Scale Network Centric Distributed Systems provides in depth coverage ranging from ground level hardware issues such as buffer organization router delay and flow control to the high level issues immediately concerning application or system users including parallel programming middleware and OS support for such computing systems Arranged in five parts it explains and analyzes complex topics to an unprecedented degree Part 1 Multicore and Many Core Mc Systems on Chip Part 2 Pervasive Ubiquitous Computing and Peer to Peer Systems Part 3 Wireless Mobile Networks Part 4 Grid and Cloud Computing Part 5 Other Topics Related to Network Centric Computing and Its Applications Large Scale Network Centric Distributed Systems is an incredibly useful resource for practitioners postgraduate students postdocs and researchers

Computational Intelligence in Digital and Network Designs and Applications Mourad Fakhfakh, Esteban Tlelo-Cuautle, Patrick Siarry, 2015-07-14 This book explains the application of recent advances in computational intelligence algorithms design methodologies and synthesis techniques to the design of integrated circuits and systems It highlights new biasing and sizing approaches and optimization techniques and their application to the design of high performance digital VLSI radio frequency and mixed signal circuits and systems This second of two related volumes addresses digital and network designs and applications with 12 chapters grouped into parts on digital circuit design network optimization and applications It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits

Data Storage Florin Balasa, 2010-04-01 The book presents several advances in different research areas related to data storage from the design of a hierarchical memory subsystem in embedded signal processing systems for data intensive applications through data representation in flash memories data recording and retrieval in conventional optical data storage systems and the more recent holographic systems to applications in medicine requiring massive image databases

Algorithms and Architectures for Parallel Processing Yongxuan Lai, Tian Wang, Min Jiang, Guangquan Xu, Wei Liang, Aniello Castiglione, 2022-02-22 The three volume set LNCS 13155 13156 and 13157 constitutes the refereed proceedings of the 21st International Conference on Algorithms and Architectures for Parallel Processing ICA3PP 2021 which was held online during December 3 5 2021 The total of 145 full papers included in these proceedings were carefully reviewed and selected from 403 submissions They cover the many dimensions of parallel algorithms and architectures including fundamental theoretical approaches practical experimental projects and commercial components and systems The papers were organized in topical sections as follows Part I LNCS 13155 Deep learning models and applications software systems and efficient algorithms edge computing and edge intelligence service dependability and security algorithms data science Part II LNCS 13156 Software systems and efficient

algorithms parallel and distributed algorithms and applications data science edge computing and edge intelligence blockchain systems deep learning models and applications IoT Part III LNCS 13157 Blockchain systems data science distributed and network based computing edge computing and edge intelligence service dependability and security algorithms software systems and efficient algorithms Mobile 3D Graphics SoC Hoi-Jun Yoo, Jeong-Ho Woo, Ju-Ho Sohn, Byeong-Gyu Nam, 2010-04-27 The first book to explain the principals behind mobile 3D hardware implementation helping readers understand advanced algorithms produce low cost low power SoCs or become familiar with embedded systems As mobile broadcasting and entertainment applications evolve there is increasing interest in 3D graphics within the field of mobile electronics particularly for handheld devices In Mobile 3D Graphics SoC Yoo provides a comprehensive understanding of the algorithms of mobile 3D graphics and their real chip implementation methods 3D graphics SoC System on a Chip architecture and its interaction with embedded system software are explained with numerous examples Yoo divides the book into three sections general methodology of low power SoC design of low power 3D graphics SoC and silicon implementation of 3D graphics SoCs and their application to mobile electronics Full examples are presented at various levels such as system level design and circuit level optimization along with design technology Yoo incorporates many real chip examples including many commercial 3D graphics chips and provides cross comparisons of various architectures and their performance Furthermore while advanced 3D graphics techniques are well understood and supported by industry standards this is less true in the emerging mobile applications and games market This book redresses this imbalance providing an in depth look at the new OpenGL ES The Standard for Embedded Accelerated 3D Graphics and shows what these new embedded systems graphics libraries can provide for 3D graphics and games developers *Advances in Computers* Suyel Namasudra, 2022-02-04 Advances in Computers Volume 124 presents updates on innovations in computer hardware software theory design and applications with this updated volume including new chapters on Traffic Load Aware Virtual Channel Power gating in Network on Chips An Efficient DVS Scheme for On chip Networks A Power Performance Balanced Network on Chip for Mixed CPU GPU Systems Routerless Networks on Chip Routing Algorithm Design for Power and Temperature Aware NoCs Approximate Communication for Energy Efficient Network on Chip Power Efficient NoC Design by Partial Topology Reconfiguration The Design of a Deflection based Energy efficient On chip Network and Power Gating in Networks on Chip Contains novel subject matter that is relevant to computer science Includes the expertise of contributing authors Presents an easy to comprehend writing style Advances in Communication, Devices and Networking Bikash Sharma, Dinh-Thuan Do, Samarendra Nath Sur, Chuan-Ming Liu, 2024-10-18 This book covers recent trends in the field of devices wireless communication and networking It gathers selected papers presented at the 7th International Conference on Communication Devices and Networking ICCDN 2024 which was organized by the Department of Electronics and Communication Engineering Sikkim Manipal Institute of Technology Sikkim India on 19 20 January 2024 Gathering cutting

edge research papers prepared by researchers engineers and industry professionals helps young and experienced scientists and developers alike to explore new perspectives and offers them inspirations on how to address real world problems in the areas of electronics communication devices and networking Nature-Inspired Networking Phan Cong-Vinh,2018-02-13

Nature inspired includes roughly speaking bio inspired physical inspired social inspired and so on This book contains highly original contributions about how nature is going to shape networking systems of the future Hence it focuses on rigorous approaches and cutting edge solutions which encompass three classes of major methods 1 Those that take inspiration from nature for the development of novel problem solving techniques 2 Those that are based on the use of networks to synthesize natural phenomena and 3 Those that employ natural materials to compute or communicate **Architecture of Computing**

Systems - ARCS 2012 Andreas Herkersdorf,Kay Römer,Uwe Brinkschulte,2012-02-09 This book constitutes the refereed proceedings of the 25th International Conference on Architecture of Computing Systems ARCS 2012 held in Munich Germany in February March 2012 The 20 revised full papers presented in 7 technical sessions were carefully reviewed and selected from 65 submissions The papers are organized in topical sections on robustness and fault tolerance power aware processing parallel processing processor cores optimization and communication and memory *Solid State Circuits*

Technologies Jacobus Swart,2010-01-01 The evolution of solid state circuit technology has a long history within a relatively short period of time This technology has lead to the modern information society that connects us and tools a large market and many types of products and applications The solid state circuit technology continuously evolves via breakthroughs and improvements every year This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology The book is composed of 22 chapters written by authors coming from 30 different institutions located in 12 different countries throughout the Americas Asia and Europe Thus reflecting the wide international contribution to the book The broad range of subjects presented in the book offers a general overview of the main issues in modern solid state circuit technology Furthermore the book offers an in depth analysis on specific subjects for specialists We believe the book is of great scientific and educational value for many readers I am profoundly indebted to the support provided by all of those involved in the work First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book *Power Distribution Networks in High Speed Integrated Circuits* Andrey Mezhiba,Eby G.

Friedman,2012-12-06 Distributing power in high speed high complexity integrated circuits has become a challenging task as power levels exceeding tens of watts have become commonplace while the power supply is plunging toward one volt This book is dedicated to this important subject The primary purpose of this monograph is to provide insight and intuition into the behavior and design of power distribution systems for high speed high complexity integrated circuits

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